Nominee: ANSYS, Inc.

Representative: Vic Kulkarni, Vice President and Chief Strategist

Vic Kulkarni is the vice president and chief strategist, Office of CTO, at ANSYS. Vic is responsible for steering the business, technology, marketing and product strategy at Semiconductor Business Unit, connecting the dots from chip-package-system design software solutions with ANSYS multi-physics simulation technology and machine learning to address challenges faced by multiple verticals, ranging from connectivity, 5G, autonomous, AI, HPC and IoT.

Vic was a co-founder, President and CEO of Sequence Design focused on EDA solutions for power and energy efficient chip designs. Sequence Design merged with ANSYS in 2009. He has held engineering and senior management positions at a number of leading semiconductor and EDA companies in the Silicon Valley for many years.

Vic has a MSEE in Solid State Electronics from University of Cincinnati. In 2007 the University honored him with the "Distinguished Alumnus Award. He has a B. Tech in Electrical Engineering from Indian Institute of Technology (IIT), Bombay.

Vic is uniquely qualified to be a valuable member of the Si2 Board due to his deep experience in both semiconductor and EDA industries and vertical market trends and roadmap. He is passionate about addressing the emerging multi-physics, multi-domain challenges in 7nm and below technology nodes, and believes that Si2 will be able to play an important role in driving the big data compute and machine learning platform standards with industry collaboration for customer success in this exciting growth opportunity ahead.

Nomination Statement: ANSYS, Inc.

ANSYS develops, markets and supports engineering simulation software used to predict how product designs will behave in real-world environments ranging from a rocket launch, flying an airplane, driving a car, using a computer, touching a mobile device, crossing a bridge, or putting on wearable technology.

For semiconductor and electronic systems design, compute-intensive pervasive simulation coupled with machine learning is critical to solve multiphysics challenges of power, performance, thermal, variability, timing, electromagnetics and reliability challenges across multiple domains of chip, package, and system (CPS). The phases of product ideation, design, validation, manufacturing, deployment to product life cycle management require an eco-system of partners, and inter-operability standards, especially as we move to 7nm and below technology nodes, to ensure time to results and PPA goals. ANSYS strongly believes in collaboration, competence and commitment of partners to enable customer success and supports the mission of Si2.

Nominee: Cadence Design Systems

Representative: Stan Krolikoski, Fellow, Strategic Alliances

Stan Krolikoski is a Distinguished Engineer at Cadence, reporting to Cadence's Senior VP of Marketing. He is responsible for all EDA Standards activities for Cadence, and also manages the relationships between Cadence and other EDA vendors through the Connections program. He has more than 30 years in the EDA industry and has served in executive roles in multiple EDA companies and Standards organizations.

Following engineering leadership roles at Honeywell as Senior Manager and IBM as Advisory Engineer, Stan worked as Vice President of Engineering at CLSI, one of the earliest VHDL companies. CLSI was acquired by Compass Design Automation, where Stan became Senior Fellow and later Chief Technologist. After leaving Compass, Stan joined Cadence, where he held multiple roles ranging from Senior Architect to Vice President of Marketing of the System-Level Design Group. He later left Cadence to become CEO of Chipvision AG, an Oldenburg, Germany-based firm that focused on power-aware synthesis. In 2007, he returned to Cadence in his current role.

From a standards perspective, Stan was leader of the original EDA standards Group, the IEEE 1076 VHDL Working Group, and subsequently became Vice Chair and later the Chair of VHDL International. He also served on the Board of Directors of Open Verilog International. He was one of the founders of the Open SystemC International Group, and served as Chair and later the Treasurer of that body. Stan is one of the co-founders of Accellera, and currently serves as a member of its Board of Directors and as Secretary of the Board. He also was one of the co-founders of the IEEE Design Automation Standards Committee (DASC) and has been its chair for the past 7 years.

Stan has been given multiple awards by various standards organizations, including a charter membership in the "Golden Core" group of the IEEE Computer Society, the Accellera Leadership Award, and the IEEE Ron Waxman award.

Nomination Statement: Cadence Design Systems

Cadence develops electronic design automation (EDA) software and hardware. It licenses software, sells or leases hardware technology and provides engineering and education services throughout the world to help manage and accelerate electronics product development processes.

Nominee: GLOBALFOUNDRIES

Representative: Richard Trihy, Vice President of Design Enablement

Richard Trihy is Vice president, Design Infrastructure, GLOBALFOUNDRIES. In this role Richard is responsible for the enablement and provision of PDKs, models and EDA design flows for for GLOBALFOUNDRIES customers and partners.

Prior to GLOBALFOUNDRIES, he was Director of R&D at Synopsys and Group Director R&D at Cadence Design Systems. He obtained B.S. and M.S. degrees in Electrical Engineering from University College Cork, Ireland, and a Ph.D. degree in Electrical and Computer Engineering from Carnegie Mellon, Pittsburgh.Richard has led development teams in Analog/Mixed Signal and RF design tools at Cadence where he represented Cadence on Verilog-A, Verilog-AMS and IEEE VHDL-AMS industry standards committees. At Synopsys, Richard led development teams in the Implementation Group and was founding chairman of the Si2 Liberty TAB.

With his broad background and over 20 years of experience in Design methodology, semiconductor and EDA he will be able to contribute to the development of useful EDA standards**.**

Nomination Statement: GLOBALFOUNDRIES

GLOBALFOUNDRIES is the world's first full-service semiconductor foundry with a truly global footprint. Launched in March 2009, the company has quickly achieved scale as one of the largest foundries in the world, providing a unique combination of advanced technology and manufacturing to more than 150 customers. With operations in Singapore, Germany and the United States, GLOBALFOUNDRIES is the only foundry that offers the flexibility and security of manufacturing centers spanning three continents.

The company's 300mm fabs and 200mm fabs provide the full range of process technologies from mainstream tothe leading edge. This global manufacturing footprint is supported by major facilities for research, development and design enablement located near hubs of semiconductor activity in the United States, Europe and Asia. For more information, visit http://www.globalfoundries.com.

Nominee: Google

Representative: Roger Carpenter, Hardware Engineer

Roger Carpenter is a Google hardware engineer with more than years 30 of experience in electronic design automation and chip design.

Before joining Google, Roger held executive roles at three EDA firms: Magma Design Automation, Javelin Design Automation and Envis. His design experience includes positions at Wave Computing, Broadcom, Chromatic Research and Xilinx.

A holder of more than a dozen patents, Roger received a Bachelor's and Master's of Electrical Engineering and Computer Science from the Massachusetts Institute of Technology**.**

Nomination Statement: Google LLC

Google LLC is an American multinational technology company that specializes in Internet-related services and products, which include online advertising technologies, search engine, cloud computing, software, and hardware. The hardware includes the Tensor Processing Unit (TPU) which is an AI accelerator application-specific integrated circuit (ASIC) developed by Google specifically for neural network machine learning. Its headquarters are in Mountain View, California.

Nominee: IBM

Representative: Leon Stock, Vice President, EDA

Dr. Leon Stok is currently Vice President of EDA at IBM and is responsible for delivering and supporting productive and effective design methodologies for all IBM design teams. This group develops design tools and design methods and provides both tools and supports experts to the entire silicon and system design community. Leon has a vision to take the CAD industry to platform level and sees a crucial role for Si2 to play in this evolution.

Prior to this he held positions as Director of EDA, Executive Assistant to IBM's Senior Vice President of Technology and Intellectual Property and executive assistant to IBM's Senior Vice President of the Technology group. Leon has been involved in the research and development of EDA tools for more than twenty years.

Leon studied electrical engineering at Eindhoven University of Technology, the Netherlands, from which he graduated with honors in 1986. He obtained a Ph.D. degree from Eindhoven University in 1991. Leon Stok worked at IBM's Thomas J. Watson Research Center as part of the team that developed BooleDozer, the IBM logic synthesis tool. Subsequently he managed IBM's logic synthesis group, and lead all of IBM's design automation research as the Senior Manager Design Automation at IBM Research from 1999-2004.

Leon has published over fifty papers on many aspects of high level, architectural and logic synthesis, low power design, placement driven synthesis and on the automatic placement and routing for schematic diagrams. He was elected an IEEE fellow for the development and application of high-level and logic synthesis algorithms. With a diverse background and a passion to develop efficient design platforms, he will be able to contribute strongly to the development and promotion of useful EDA standards.

Nomination Statement: IBM

The systems and products designed by IBM rely heavily on the ability to quickly and accurately design complex silicon functions. Over the last decades the silicon content of IBM systems has increased drastically. This requires a significant improvement in designer productivity. Something that can only be realized by design tools that are operating in flows that are as seamless as possible Our design flows consist of a mixture of internally developed and externally acquired tools from most EDA vendors. The interoperability of this entire toolset is essential to deliver the productivity required. Therefore, IBM is a strong supporter of open EDA standards and technologies and vigorously supports the objectives of Si2.

Nominee: Intel

Representative: Rahul Goyal, Vice President, EDA

Rahul Goyal is responsible for Intel's strategic engagements with the EDA industry. His team drives Intel's EDA strategy, supplier engagements, strategic equity investments in design & CAD, standards development with industry consortia, and university research in design sciences.

Rahul has been with Intel for over 24 years, and has held several technical and management positions in software engineering and technology development. Prior to joining Intel, Rahul was a design engineer.

Rahul is a member of the board of directors of Silicon Integration Initiative (Si2). He has also served as chairman of Design Technology Council (DTC), an industry think tank, and as an observer on the board of directors of several Intel Capital portfolio companies.

Rahul holds a Master's degree in Computer Engineering from Syracuse University, and a Bachelor's degree (with honors) in Electrical Engineering from BITS, Pilani, in India.

Nomination Statement: Intel

The systems and products designed by Intel Corporation rely heavily on the ability to quickly and accurately design complex silicon functions. Over the last ten years, not only has the silicon content of Intel systems increased exponentially, but a migration from a design environment of internally developed EDA tools to a large number of EDA tools acquired commercially has also occurred. Given that Intel subscribes to a multiple EDA vendor philosophy and uses a cross-section of tools from EDA vendors, the interoperability of those tools is essential for effective silicon design. Therefore, Intel is a strong supporter of open EDA standards and technologies and vigorously supports the objectives of Si2.

Nominee: Mentor Graphics, a Siemens Business

Representative: Mick Tegethoff, Director of Marketing, AMC IC Verification Solutions

Dr. Mick Tegethoff, is the Director of Product Marketing for Analog/ Mixed-Signal/RF IC Verification Solutions at Mentor, a Siemens Business. Prior to joining Mentor, Mick was the Director of Technical and Product Marketing at Berkeley Design Automation (BDA), where he was responsible for product and strategic marketing of the company's circuit simulation and transistor-level noise analysis products.

During this period, BDA received a Red Herring Hot 100 award and appeared twice on the Deloitte Technology Fast 500, which recognizes the fastest growing technology companies in North America by revenue growth. Mick began his career as an IC design engineer. After almost a decade at HP, with increasing engineering management responsibilities, he joined Celestica where he expanded into manufacturing, product operations, and management.

Mick then joined Agilent Technologies, as the Marketing Manager for IC Test Solutions, as the design for test (DFT) industry was experiencing significant growth. He then moved to Cadence where he was responsible for all marketing for DFT products. One of Mick's key professional accomplishments was the development of a patented statistical simulator for electronic product manufacturing. Mick holds a BS and MS in Electrical Engineering from the University of Arizona, a Ph.D. in Electrical Engineering from Colorado State University. He is a Senior Member of IEEE.

Nomination Statement: Mentor Graphics, a Siemens Business

Mentor Graphics Corp., a Siemens Business, is a world leader in electronic and software design solutions, providing products, consulting services, and award-winning support for the world's most successful electronic, semiconductor and systems companies. We are unique in providing solutions for both the hardware components (the chips and boards) and the software components (the embedded operations systems and applications/drivers that control the product's operation). Since the company's inception, Mentor has focused on providing leading tools for the design and verification of electronic systems with a focus on best-in-class solutions. Mentor strongly promotes open design flows that enable our customers to build flows combing best-in-class products. The interoperability of EDA tools has been central to this mission. Mentor is a strong supporter of open EDA standards.

Nominee: Qualcomm Technologies

Representative: Udi Landen, Vice President of Engineering

Udi Landen is Vice President of Engineering at Qualcomm Technologies, Inc. In his current role, Udi provides technical, management and business leadership for engineering teams at various international sites that focus on mobile and computing design enablement and CAD methodology automation roadmaps.

Prior to joining Qualcomm in 2013, Udi held executive and leadership roles at Altera Corp., Mercury Interactive and Cadence Design Systems. He is a graduate of the Technion, Israel Institute of Technology.

Nomination Statement: Qualcomm Technologies

Qualcomm CDMA Technologies (QCT) is the world's largest fabless semiconductor producer and the largest provider of wireless chipset and software technology, which powers the majority of all 3G devices commercially available today. We are redefining the experience of wireless mobility by applying our unmatched legacy of wireless innovation to enable new generations of increasingly powerful mobile handsets, computers and consumer electronics devices.

With expertise honed from more than 25 years of wireless industry leadership, QCT continues to break new grounds, innovating across multiple technologies such as CPU, GPU, Modem, GPS, connectivity, etc., and as a result iscontinually expanding our product offerings.

Nominee: Samsung Electronics

Representative: Seungbum Ko, Vice President, Samsung Electronics Design Technology Team

Seungbum Ko is vice president of the Samsung Electronics Design Technology Team. He is responsible for all memory design methodology activities for the Samsung memory division, and also manages the relationships between memory division and EDA vendors.

A 21-year veteran at Samsung, his expertise includes development of SDRAM, DDR, DDR2, DDR3, LPDD2, LPDDR3 and LPDDR4 devices. His internal honors include the Proud Samsung Award, the Jang Young-sil Award, and the Memory Award.

Nomination Statement: Samsung Electronics

The Samsung Electronics System-LSI Business Division has three Business Groups: Foundry Business, SOC Business, and LSI Business. We need to prepare a seamless design flow with diverse tools from different EDA vendors for not only internal designs (SOC and LSI) but also outside customers (Foundry). Therefore, interoperability of these entire tool sets is essential to deliver the productivity required. Moreover, because we need to prepare the design infrastructure for most advanced process nodes continuously, we need to develop an industry standard flow.

Nominee: Synopsys

Representative: David MeMaria, Vice President Corporate Marketing

Dave DeMaria joined Synopsys in 2013 and is Vice President of Corporate Marketing. He has more than 25 years of experience in the EDA, IP and semiconductor industries.

Prior to Synopsys, he held senior executive positions at Cadence, MoSys, Apache, Optimal, Viewlogic and Zuken. Dave attended Boston University for a B.S. degree in Computer Engineering.

Nomination Statement: Synopsys

Synopsys, Inc. provides products and services that accelerate innovation in the global electronics market. As a leader in (EDA) and semiconductor intellectual property (IP), Synopsys' comprehensive, integrated portfolio of system-level, IP, implementation, verification, manufacturing, optical and field-programmable gate array (FPGA) solutions help address the key challenges designers face such as power and yield management, system-to-silicon verification and time-to-results.

These technology-leading solutions help give Synopsys customers a competitive edge in quickly bringing the best products to market while reducing costs and schedule risk. For more than 25 years, Synopsys has been at the heart of accelerating electronics innovation with engineers around the world having used Synopsys technology to successfully design and create billions of chips and systems. The company is headquartered in Mountain View, California, and has approximately 90 offices located throughout North America, Europe, Japan, Asia and India.

Synopsys continues to champion customers' requirements for interoperability throughout the EDA and semiconductor industries. Synopsys has made strong and valuable contributions of technology, manpower, and funding to a variety of organizations and initiatives that have resulted in tangible benefits to the design community. Synopsys desires to continue its involvement with Si2 as a member of the Si2 Board of Directors to serve the electronics community by bringing expertise and resources to bear upon the ongoing challenge of interoperability for IC design and manufacturing. Synopsys agrees with Si2 that through collaborative efforts, the IC industry can achieve higher levels of SoC integration, improve productivity, and reduce cost.

Nominee: Texas Instruments

Representative: Keith Greene, Distinguished Member of the Technical Staff

Dr. Keith Green is a Distinguished Member of the Technical Staff in the Analog Technology Development department, where he directs development of circuit simulation tools for front-end reliability. During his more than two decades with TI, he has had various technical and leadership roles in the area of SPICE modeling. His expertise spans a wide range of technologies such as high-voltage LDMOS, low-voltage scaled CMOS, bipolar junction.

Keith was a founder of the Compact Model Council in 1996. This international consortium is dedicated to the standardization of SPICE model formulations and modeling interfaces. Since 2012 he has been the Chairman of the CMC, and in 2013 he initiated its move to Si2 where it is now known as the Compact Model Coalition. He guided strategic university research as Chairman of the Semiconductor Research Corporation's Compact Modeling Technical Advisory Board from 2004 to 2011.

Keith has four patents, over 20 publications, and has been an invited speaker at several conferences and universities. He received Ph.D. and M.S. degrees in Electrical Engineering from the University of Florida and a B.S. degree in Electrical Engineering from the University of Delaware.

Nomination Statement: Texas Instruments

Texas Instruments Incorporated (TI) is a global semiconductor design and manufacturing company that develops analog integrated circuits (ICs) and embedded processors. The process of designing these products relies heavily on electronic design automation (EDA) tools. The accuracy of these tools is as critical as their ability to operate reliably with technology design kits developed both in-house and by commercial foundries. Therefore, TI has a strong interest in the mission of Si2 to deliver standards for improving IC design capability. As an integrated device manufacturer, TI's interests span manufacturing, design, packaging and test. As a member of the Board of Directors, TI would bring perspective on all of these aspects for a wide spectrum of technologies that include silicon for low-power to high-voltage, gallium-nitride, MEMs and sensors.

Nominee: Zuken

Representative: Humair Mandavia, Chief Strategy Officer

Humair Mandavia is the Chief Strategy Officer at Zuken and responsible for research and development in the United States. His role includes partnering with industry-leading customers to drive the latest innovation in EDA, and providing guidance for corporate and product direction.

The US R&D team is focused on supporting companies evolving to system- level design processes, and requiring multi-domain co-design of electronic systems using Zuken's CR-8000 solution.

Humair's past roles include Director of Engineering and Senior. Solutions Architect for Zuken USA.

Nomination Statement: Zuken

Zuken is a global provider of leading-edge software and consulting services for electrical and electronic design and manufacturing. Founded in 1976, Zuken has the longest track record of technological innovation and financial stability in the electronic design automation (EDA) software industry. The company's extensive experience, technological expertise and agility, combine to create world-class software solutions. Zuken's transparent working practices and integrity in all aspects of business produce long-lasting and successful customer partnerships that make Zuken a reliable long-term business partner.

Today, Zuken's product offerings include EDA solutions for Advanced Packaging and PCB design, Computer Aided Engineering (CAE), wire harness and cable design, and engineering data management solutions. With design teams shifting to a collaborative process and multi-domain co-design, Zuken is developing tools that enable concurrent implementation of chip, package, PCB, and mechanical design to help teams realize optimized quality and performance of their products.

Innovation is a way of life at Zuken. The company software specialists at its development centers in Japan, Europe and the U.S. As a result, customers benefit from the work of the largest IC packaging, PCB- and wiring-focused R&D teams of their kind. This driving force of innovation keeps Zuken at the forefront of technological advancement.