MIT Virtual Source GaN HEMT: MVSG Model Manual

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Contents

Introduction

HV-Gallium Nitride (GaN) based high electron mobility transistors (HEMTs) are starting to be used in RF and power conversion applications in industry [1]. This is because of the possibility of higher switching voltage and switching frequency with GaN HEMTs in comparison to conventional Si-FETs, which enables delivery of high power levels at high frequencies for RF applications, scaling of passive components in HV circuits resulting in high efficiency and lower footprint of power conversion boards. Compact models are necessary for designing such RF-circuits such as power amplifiers and HV-GaNFET switching converter circuits. Several compact models of GaN HEMTs have been developed for this purpose [2]. In this work the physics based compact model developed at MIT based on VS-concept [3] for these devices is discussed. Details of the Verilog-A model equations along with parameter extraction procedure are explained.

GaN HEMT: Working principle

Gallium Nitride HEMT is an attractive candidate for HV and HF applications. This is due to superior and unique properties AlGaN/GaN system such as high electron density ($\sim 1 \times 10^{13}$ cm^2), high electron mobility in two dimensional electron gas (2DEG)(~ 1500 cm^2/Vs), good thermal conductivity (~ 1.5 W/cm. K) and high breakdown field (~ 3.0 MV/cm). These properties are compared with other materials and summarized in Fig.1.

Semiconductor		Si	AlGaAs/ InGaAs	InAlAs/ InGaAs	SiC	AlGaN/ GaN
Characterisitic	Unit					
Bandgap	eV	1.1	1.42	1.35	3.26	3.49
Electron mobility at 300 K	cm²/Vs	1500	8500	5400	700	1500-2200
Saturated (peak) electron velocity	$\times 10^7$ cm/s	1.0 (1.0)	1.3 (2.1)	1.0 (2.3)	2.0 (2.0)	1.3 (2.1)
Critical breakdown field	MV/cm	0.3	0.4	0.5	3.0	3.0

Fig.1: Table showing material properties. GaN shows a combination of high electron mobility, electron velocity and breakdown field [2]

The above-mentioned properties of GaN material systems results in superior switching figure-of-merit ($BV^2/R_{on}Q_G$) for FETs used in 600-1200V applications. The plot of BV vs. R_{on} of the three competing material systems for this voltage regime is shown in Fig. 2. As can be seen, for a given BV, the R_{on} of GaN beats the Si and SiC limits and it is this combination of good transport properties and high breakdown field that opens up the RF and HV application domain to GaN HEMTs.

GaN-based HEMTs, similar to other HEMTs, are field effect transistors having a hetero-junction formed between two materials (in this case AlGaN and GaN) with different lattice constants. A schematic of the device structure is shown in Fig. 3a. The difference in electron affinity (χ) and band gap (E_g) results in the formation of a nearly triangular potential well at the interface on the GaN side where electrons can be confined and form a 2DEG as shown in Fig. 3b. However, the cause for the 2DEG is different from other HEMT devices.

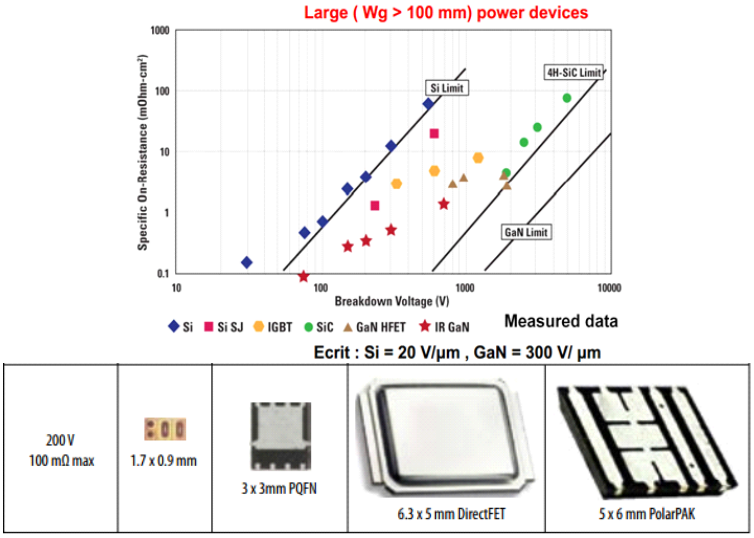


Fig.2: (a) BV vs. Ron of Si, SiC and GaN material system highlighting the superior DC-FoM of GaN HEMTs that makes (b) high frequency makes smaller circuit footprint possible [2].

The polar nature of the AlGaN/GaN system results in spontaneous polarization and in addition, the difference in lattice constants of the two layers results in piezoelectric polarization. In GaN HEMTs, the 2DEG is not induced by doping but instead by donor-like surface states on the AlGaN layer facilitated by spontaneous and piezoelectric electric field in AlGaN layer.

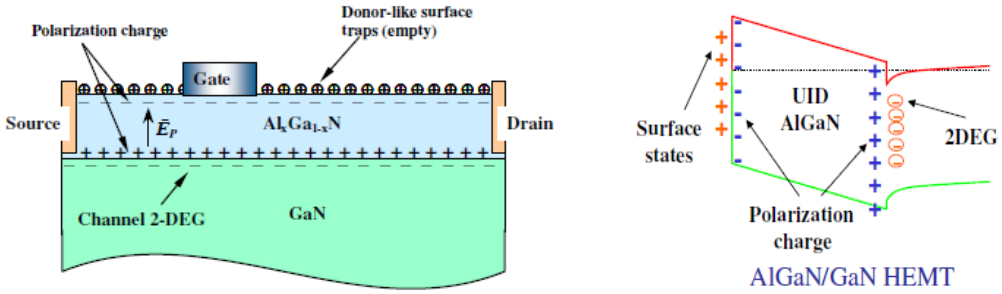


Fig.3: (a) Device structure schematic. (b) Band diagram of heterostructure showing different types of charges

Confinement of electrons in the quantum well and absence of dopants in the channel result in high mobility and peak velocity. Operation of the device requires a gate terminal to modulate the 2DEG and hence drain to source current (I_{DS}). Since the 2DEG exists due to the heterostructure, a negative gate voltage is required to deplete it under the gate and prevent current flow. Therefore, GaN HEMTs without special gate stack engineering are normally-on (depletion-mode, D-mode) devices. Further details on the working principle can be found in [2]. With this basic understanding of device operation, we can look at the approach taken by the MIT Virtual Source GaNFET (MVSG) model to capture the device behavior under operating bias voltage.

MVSG Model

Typical device structure of GaN HEMT is shown in Fig. 4a. There are five distinct regions of the device, which require modeling attention. There is the intrinsic transistor region under the gate, where the 2DEG is modulated by the gate voltage (V_g), there are two regions next to the gate on the drain side called the field plate regions which augment breakdown voltage capability of GaN HEMTs (MVSG supports upto 4 field plates) and two access regions (these devices are not self-aligned). The access regions (between source-gate and drain-gate) are modeled as non-linear implicit-gate transistors. The MVSG model captures carrier transport in these different regions of the device with the help of sub-circuit model shown in Fig. 4b. More details of the model equations can be found in [2]. In this manual, the implementation of the model equations in Verilog-A code will be described in detail.

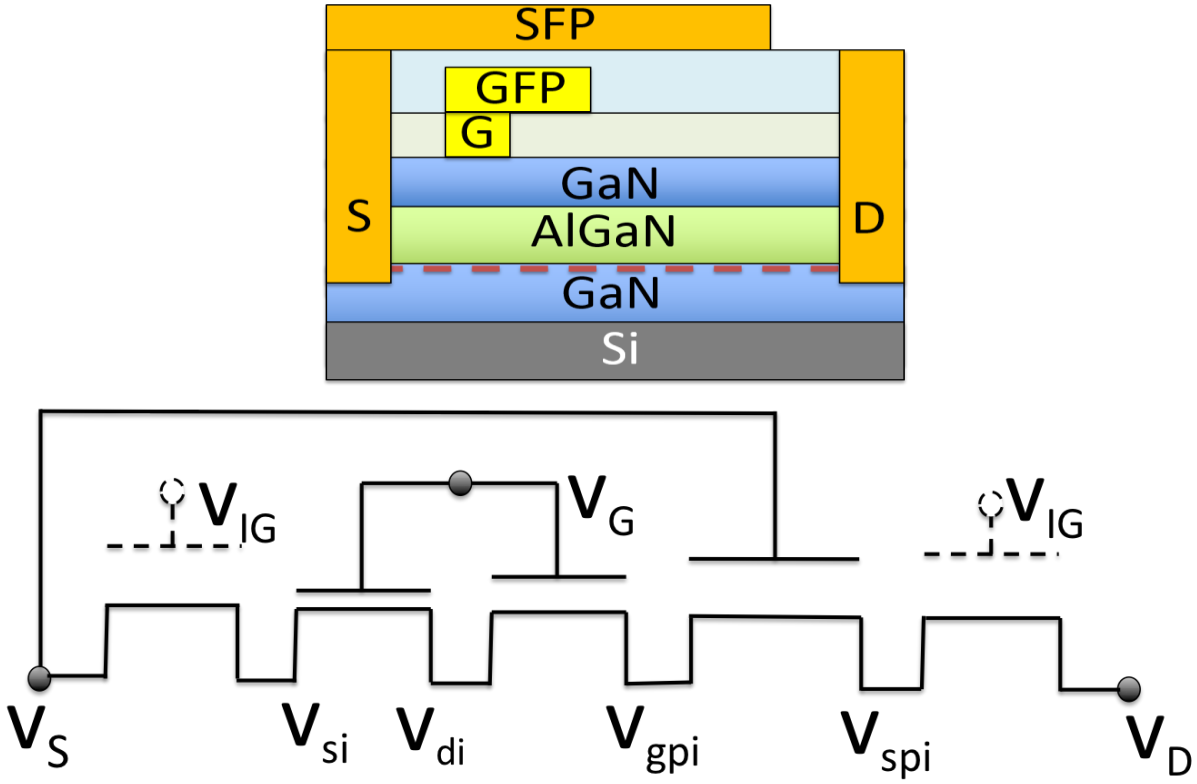


Figure 4. (a) Cross-sectional schematic of GaN HEMTs on Si. (b) The equivalent circuit for the model with intrinsic transistor, gate-field-plate, source-field-plate and implicit-gate access region transistors is shown.

The sub-circuit modeling approach shown above computes the voltage distribution in the device accurately under any bias condition and correctly captures depletion and other high voltage effects**.** The two field plate (FP) transistors (the FP with its gate connected to the gate terminal and the FP with its gate connected to the source terminal) have different V_Ts due to the dielectric used. The further the FP is from the gate edge, the more negative its V_T. This ensures that in the off-state, as V_{DS} is increased in the off-state, the field plates progressively deplete at different V_T, prevent peak-fields from reaching the critical field and hence premature device breakdown.

MVSG Model: Verilog-A implementation

1. Terminal voltage definition

The following sections will describe the Verilog-A code lines in the order they appear in the file **'mvsg_cmc.va'**. First part of the Verilog-A implementation of the MVSG model involves the definition of terminal voltages for each sub-circuit element shown in Fig. 5.

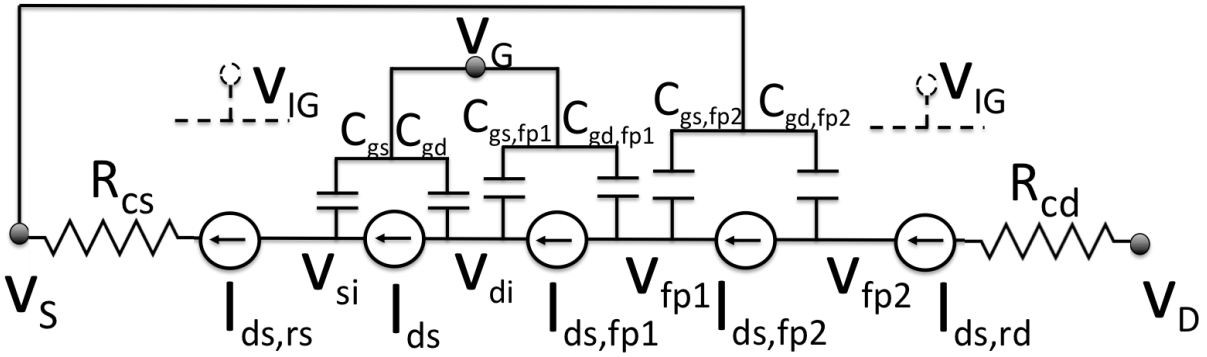


Figure 5. The equivalent circuit for the model showing all the intrinsic and extrinsic nodes along with intrinsic transistor, field plate regions, implicit-gate access region transistors and contact resistances (R_{cs} and R_{cd}) is shown. The equivalent gate-source and gate-drain voltages of each transistor element should be defined in the Verilog-A version of the model.

Figure 5. shows the MVSG GaN HEMT schematic where external terminals are labeled as **d** (Drain), **g** (Gate) and **s** (Source) (there is no body terminal). Internal gate is same as the external one. Internal drain terminal of the intrinsic transistor is labeled as **di**, while internal source terminal is labeled as **si**. In addition, there are source and drain contact resistances which require additional intrinsic nodes: **src** and **drc**. **src** forms the intrinsic source node of source-implicit-gate transistor and **drc** forms the intrinsic drain node of the drain-implicit-gate transistor. The additional nodes are **fp1** and **fp2** corresponding to the drain nodes of GFP and SFP transistors respectively. The model accommodates upto 4 field plates and so there are two additional internal nodes **fp3** and **fp4**, which are collapsed since there are no more than 2 FPs in the benchmarked device. Users can activate them by using non zero gate lengths for these additional FP transistors.

Analog function: sd_dir

```
analog function real sd_dir;
inout vgsout,vdsout;
input vgsin,vgdin,vdsin;
real  vgsout,vdsout,vgsin,vgdin,vdsin;
real  vgsType, vgdType, vdsType;
begin
vgsType    = vgsin * type;
vgdType    = vgdin * type;
vdsType    = vdsin * type;
vgsout     = vgsType;
vdsout     = vdsType;
sd_dir      = 1.0;
end
endfunction
```

The analog function sd_dir computes the gate-source, gate-drain and drain-source voltages for each transistor region shown in Fig. 5. The model is inherently source-drain symmetric for each transistor region even though the GaN HEMT is inherently an asymmetric device due to different source and drain access region lengths. Ensuring source-drain symmetry ensures that the code is robust around V_{DS}=0 V.

Intrinsic transistor

The intrinsic transistor voltage definitions is done by the function call below, where vgsi and vdsi are the gate-source and drain-source voltages respectively

```
dir          = sd_dir(vgsi,vdsi,V(gi,si),V(gi,di),V(di,si));
```

Source and drain implicit-gate transistors

The source and drain access regions do not have actual gate terminal. The implicit gate terminal (denoted by V_{IG} in Fig. 5) is non-existent and is only linked to the sheet resistance (Rsh) and carrier mobility (mu0) in these regions through an additional fitting parameter Cgrs (Cgrd). More details can be found in [2]. The terminal voltages for these implicit-transistors are defined in a way similar to that of the intrinsic transistor region as shown below:

Source implicit-gate transistor

```
vigs    = vtors + 1.0 / (rsh * cgrs * mu0) + min(V(d), V(s));
dirrs   = sd_dir(vgsrs,vdsrs, (vigs - V(src)),(vigs - V(si)),V(si,src));
```

Drain implicit-gate transistor

```
vigd    = vtord + 1.0 / (rsh * cgrd * mu0) + min(V(d), V(s));
dirrd   = sd_dir(vgsrd,vdsrd, (vigd - V(fp4)),(vigs - V(drc)),V(drc,fp4));
```

Field plate transistors

The field plates are similar to the intrinsic gated transistor and are present between gate and drain terminals. Using non-zero gate lengths can activate the field plate regions and **flagfpx** (x=1 to 4) parameter can be used to define the gate terminal as either gate-connected or source-connected. The voltage definitions are then based on the value of flagfp1 as shown below for FP1. The other 3 FPs are defined similarly.

```
if (flagfp1 == 1) begin
  dirfp1    = sd_dir(vgsfp1,vdsfp1,V(gi,di),V(gi,fp1),V(fp1,di));
  vcfp1     = type * V(s,di);
end else begin
  dirfp1    = sd_dir(vgsfp1,vdsfp1,V(s,di),V(s,fp1),V(fp1,di));
  vcfp1     = type * V(gi,di);
end
vbfp1       = type * V(b,di);
```

2. Temperature dependence

HV-GaN HEMTs have high power dissipation due to high current densities (few A/mm) and poor thermal conductivity of the Si substrate. Therefore GaN compact models must incorporate temperature dependence on carrier transport parameters such as mobility and carrier velocity. Self-heating is captured in the model by employing a thermal node (**dt**). Both change in temperature due to change of ambient temperature and due to device self-heating is included. The temperature dependence of mobility (muf), velocity (vx), threshold voltage (vtof), contact resistance (rs and rd) and subthreshold slope (S, through phit) are captured by the following equations:

```
  tambk       = $temperature;
  tsh         = Temp(dt);
  tdut        = tambk + tsh;
  rd          = ( rcd / weff ) *  ( 1 + rct1 *  ( tdut-tnomk ) + rct2 *  ( tdut - tnomk ) *  ( tdut -
tnomk )) / ngf;
  rs          = ( rcs / weff ) *  ( 1 + rct1 *  ( tdut-tnomk ) + rct2 *  ( tdut - tnomk ) *  ( tdut -
tnomk )) / ngf;
  phit        = `P_K * tdut / `P_Q;
  muf         = mu0 / (( pow(( tambin / tnomin ),epsilon )));
  vx          = vel0 * (( 1.0 + vzeta * tnomin ) / ( 1.0 + vzeta * tambin ));
 vtof         = vto + vtzeta * ( tambin - tnomin );
  phit        = $vt(T);
```

The temperature rise in the device caused because of self-heating is captured using an RC (rth and cth) network connected to the thermal node. The power dissipation in the device is captured as the sum of the product of voltage drop and current in each region of the device as follows:

```
  if (rth !=0) begin
    pdiss       = -( ids * V(di,si) + idsrd * V(drc,fp4) + idsrs * V(si,src) +  idsfp1 * V(fp1,di) +
idsfp2 * V(fp2,fp1) + idsfp3 * V(fp3,fp2) + idsfp4 * V(fp4,fp3) + V(src,s) * V(src,s) / rs +
V(drc,d) * V(drc,d) / rd);
    Pwr(dt)     <+ ddt( (cth + mycmin) * Temp(dt));
    Pwr(dt)     <+ pdiss;
    Pwr(dt)     <+ Temp(dt) / rth;
  end
  else
    Pwr(dt)     <+ Temp(dt) * 1e9;
```

3. Transistor drain current formulation

In the MVSG model, the intrinsic, access region and FP regions are assumed to be long enough (compared to mean free path) so that carrier transport is drift-diffusion (DD) based. So the implicit-gate model for these regions are essentially non-ballistic-channel transistor models which are suitable for channel lengths longer than ~500nm. The model equations described below are generic in nature and are applicable to each transistor region of the HEMT with their own parameters. For the implicit-gate transistors, gate overdrive voltage is linked to the sheet resistance as given in [7]. The rest of the formulation is that of a conventional mobility limited/saturation velocity limited transport FET model. The DD channel model equations employed in MVSG model for these regions assume the band profile as shown in Fig. 6.

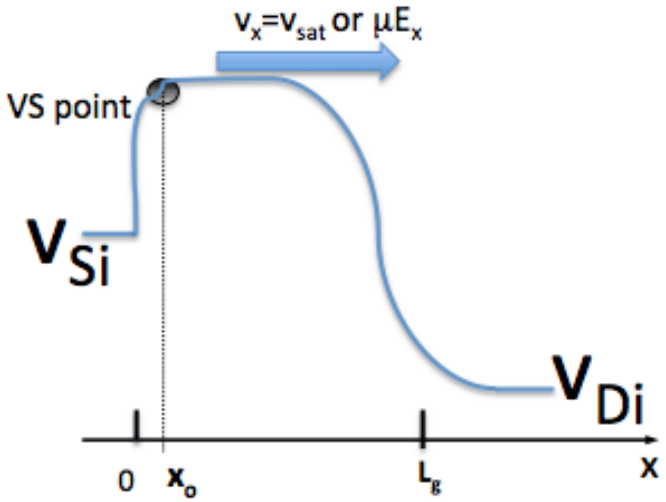


Fig. 6: Conduction band profile assumed in DD- channel transistor model under drain bias.

The current is given by the product of charge and velocity at the VS point (for that matter at any point in the channel, current is the product of local charge and velocity) but while the charge at the VS point is still the same as given by (2) in [8], the velocity at the VS point is no longer a simple constant, bias-independent quantity as in ballistic (refer to MVSG-RF model) HEMTs. In long channels, transport is governed by drift/diffusion (DD) and the carrier velocity at any point in the channel is dependent on the local field as $v_x = \mu_{eff} E_x$. The current is evaluated using the following procedure:
The master equation for drift current is given by

$$I_D/W = Q_{ix} v_x = Q_{ix} \mu_{eff} E_x = Q_{ix} \mu_{eff} \frac{d\psi}{dx} \qquad (1)$$

Here ψ is the potential at location x. For the charge-based simplified all-region model, the channel layer charge is expressed as given in [9] and

$$\frac{dQ_{ix}}{d\psi} = C_{inv} \qquad (2)$$

Using Caughey and Thomas model [4] for carrier velocity dependence on field, the effective mobility is given by

$$\mu_{\text{eff}} = \frac{\mu}{\left(1+\left(\frac{\frac{d\psi}{dx}}{L_g{}^{\nu}/\mu}\right)^{\beta}\right)^{1/\beta}} \qquad (3)$$

This formulation assumes that the carrier velocity profile with field is similar to that of Si i.e. carrier velocity increases with field and saturates at saturation velocity. It takes the form of drift velocity in strong accumulation and diffusion velocity in weak accumulation. In addition, in strong accumulation the velocity 'v' includes GaN specific effects such as self-heating and scattering whose functions are multiplied to bias-independent saturation velocity (v_{sat0}). Using (2-3), (1) can be rewritten as

$$I_D/W = Q_{ix}\frac{\mu}{\left(1+\left(\frac{dQ_{ix}}{C_{inv}L_g{}^{\nu}/\mu dx}\right)^{\beta}\right)^{1/\beta}}\frac{dQ_{ix}}{C_{inv}dx} \qquad (4)$$

Using current continuity and assuming $\frac{dQ_{ix}}{dx} = \frac{Q_{is}-Q_{id}}{L_g}$ in the denominator of (4), we can integrate the above expression from x=0 to x=L_g and $Q_{ix} = Q_{is}$ to $Q_{ix} = Q_{id}$. The resulting current is given by

$$I_D/W = \frac{\mu}{2C_{inv}L_g}\frac{{Q_{is}}^2-{Q_{id}}^2}{\left(1+\left(\frac{Q_{is}-Q_{id}}{C_{inv}L_g{}^{\nu}/\mu}\right)^{\beta}\right)^{1/\beta}} \qquad (5)$$

Here v is the carrier velocity combining strong and weak accumulation regimes, as discussed below. In order to make the current expression look similar to that of VS model expression in (4) in [8], the previous expression (5) can be reformulated as follows

$$\frac{I_D}{W} = v\frac{1}{2C_{inv}V_{DSAT}}\frac{{Q_{is}}^2-{Q_{id}}^2}{\left(1+\left(\frac{Q_{is}-Q_{id}}{C_{inv}V_{DSAT}}\right)^{\beta}\right)^{\frac{1}{\beta}}} = v\frac{Q_{is}+Q_{id}}{2}F_{vsat} \qquad (6)$$

Where $F_{vsat} = \frac{\frac{Q_{is}-Q_{id}}{C_{inv}V_{DSAT}}}{\left(1+\left(\frac{Q_{is}-Q_{id}}{C_{inv}V_{DSAT}}\right)^{\beta}\right)^{\frac{1}{\beta}}}$ and V_{DSAT} is similar to that in (5) in [8]. V_{DSAT} must account for both strong and weak accumulation regimes and so should v. To do this we follow a similar procedure as in (5) in [8] and is shown below.

$$V_{DSAT} = V_{DSATS}(1-F_f) + 2n\varphi_t F_f \quad \text{and } V_{DSATS} = \frac{v_{sat}L_g}{\mu} \qquad (7a)$$

$$v = v_{sat}(1-F_f) + 2\varphi_t\frac{\mu}{L_g}F_f \quad (7b)$$

v_{sat} is what we call the GaN 'saturation velocity' which is similar to the saturation velocity in Si.

In the long channel limit, where transport is mobility limited (Non-velocity saturation: NVsat), $V_{DSAT} \gg \frac{Q_{is}-Q_{id}}{C_{inv}}$ which means $F_{vsat} = \frac{Q_{is}-Q_{id}}{C_{inv}V_{DSAT}}$ and (6) reduces to

$$\frac{\mathrm{I_D}}{W} = v\frac{{Q_{is}}^2-{Q_{id}}^2}{2C_{inv}V_{DSAT}} \qquad (8)$$

(8) has a form very similar to the EKV model used for long channel MOSFETs. In shorter channel velocity saturation (Vsat) limit, $V_{DSAT} \ll \frac{Q_{is}-Q_{id}}{C_{inv}}$ and $F_{vsat} = 1$ which leads to a simple current expression

$$\frac{\mathrm{I_D}}{W} = v\frac{Q_{is}+Q_{id}}{2} \qquad (9)$$

This expression for current is of the same form as VS model expression of (4) in [8] except that the charge here is the average of source-end and drain-end charges while in the VS Model it is just the charge at the VS point. The expression for charges at the source-end and drain-end is similar to that in (2) in [8] and are given by (10)

$$Q_{is} = 2C_{inv}\,n\,\varphi_t ln\left(1+exp\frac{V_{GDi}-\mathrm{Vxs}-(V_T-\alpha\varphi_t F_f)}{2n\,\varphi_t}\right)\; Q_{id} = 2C_{inv}\,n\,\varphi_t ln\left(1+exp\frac{V_{GSi}-\mathrm{Vxd}-(V_T-\alpha\varphi_t F_f)}{2n\,\varphi_t}\right)$$

Here, complete S/D symmetry is achieved using the above charge formulation. The terms Vxs and Vxd are in turn required to include velocity-saturation effects that will be explained in the next-sub section and are given here:

$$V_{XS} = \frac{V_{DSi}}{\left(1+\left(V_{DSi}/V_{DSAT}\right)^{\beta}\right)^{1/\beta}}\;;\; V_{XD} = \frac{-V_{DSi}}{\left(1+\left(V_{DSi}/V_{DSAT}\right)^{\beta}\right)^{1/\beta}} \qquad (11)$$

The charge expressions above are needed to model the subthreshold regime accurately. In the subthreshold regime the above expressions are reduced to

$$Q_{is} = 2C_{inv}\,n\,\varphi_t exp\frac{V_{GSi}-(V_T-\alpha\varphi_t)}{2n\,\varphi_t}\;;\; Q_{id} = 2C_{inv}\,n\,\varphi_t exp\frac{V_{GDi}-(V_T-\alpha\varphi_t)}{2n\,\varphi_t} \qquad (12)$$

Substituting (7) and (12) in (8), the current $\mathrm{I_D}$ in subthreshold regime, where diffusion current dominates, is

$$\frac{\mathrm{I_D}}{W} = v\frac{1}{2C_{inv}V_{DSAT}}\frac{\left(2C_{inv}\,n\,\varphi_t exp\frac{V_{GSi}-(V_T-\alpha\varphi_t)}{2n\,\varphi_t}\right)^2-\left(2C_{inv}\,n\,\varphi_t exp\frac{V_{GDi}-(V_T-\alpha\varphi_t)}{2n\,\varphi_t}\right)^2}{\left(1+\left(\frac{2C_{inv}\,n\,\varphi_t exp\frac{V_{GSi}-(V_T-\alpha\varphi_t)}{2n\,\varphi_t}-2C_{inv}\,n\,\varphi_t exp\frac{V_{GDi}-(V_T-\alpha\varphi_t)}{2n\,\varphi_t}}{C_{inv}V_{DSAT}}\right)^{\beta}\right)^{\frac{1}{\beta}}}$$

$$\approx 2\varphi_t\frac{\mu}{L_g}\frac{(2C_{inv}\,n\,\varphi_t)^2}{2C_{inv}2n\varphi_t}\left(exp\frac{V_{GSi}-(V_T-\alpha\varphi_t)}{n\,\varphi_t}-exp\frac{V_{GDi}-(V_T-\alpha\varphi_t)}{n\,\varphi_t}\right)$$

$$\frac{\mathrm{I_D}}{W} = \varphi_t\frac{\mu}{L_g}\left(2C_{inv}\,n\,\varphi_t exp\frac{V_{GSi}-(V_T-\alpha\varphi_t)}{n\,\varphi_t}-2C_{inv}\,n\,\varphi_t exp\frac{V_{GDi}-(V_T-\alpha\varphi_t)}{n\,\varphi_t}\right) \qquad (13)$$

This is similar to the well-known sub threshold MOSFET diffusion current.

Transition from non-saturation to saturation current

In order to facilitate smooth transition from linear to saturation regimes under applied V_{DS} we use similar function F_{sat} as in (4) in [8]. The charge expression at the source and drain-end is modified with V_{DS} as

$$Q_{is(d)} = 2C_{inv}\, n\, \varphi_t ln\left(1 + exp\frac{V_{Gd(s)i} - (+)V_{DSAT}F_{sat} - (V_T - \alpha\varphi_t F_f)}{2n\,\varphi_t}\right) \qquad (14)$$

Where $V_{DSAT}F_{sat}$ is given by

$$V_{DSAT}F_{sat} = V_{DSAT}\frac{V_{DSi}/V_{DSAT}}{\left(1+(V_{DSi}/V_{DSAT})^{\beta}\right)^{1/\beta}} = \frac{V_{DSi}}{\left(1+(V_{DSi}/V_{DSAT})^{\beta}\right)^{1/\beta}} \qquad (15)$$

Here V_{DSAT} is as given in (7a) and $V_{DSi} = V_{Di} - V_{Si}$ is the intrinsic drain to source voltage. In the linear regime (at low V_{DSi}), $V_{DSAT}F_{sat}$ approaches V_{DiSi} and Q_{id} in (14) becomes comparable to Q_{is}. Thus, the current formulation of (5) reduces to

$$\frac{I_D}{W} = \frac{\mu}{2C_{inv}L_g}\frac{{Q_{is}}^2 - {Q_{id}}^2}{\left(1+\left(\frac{Q_{is}-Q_{id}}{C_{inv}V_{DSAT}}\right)^{\beta}\right)^{\frac{1}{\beta}}} = \frac{\mu}{2C_{inv}L_g}\left({Q_{is}}^2 - {Q_{id}}^2\right) \approx \frac{\mu Q_{is}}{C_{inv}L_g}(Q_{is} - Q_{id}) \quad (16)$$

Irrespective of V_{DSAT}, the denominator of the first expression in (16) tends to 1 as $Q_{is} - Q_{id} << C_{inv}V_{DSAT}$. Thus, transport regime (NVsat or Vsat) has no bearing on current in linear regime. More details of this model can be found in [2].

GaN specific effects

In GaN HEMTs electron velocity decreases as charge density increases due to strong electron-optical phonon interaction (scattering) and this is modeled empirically using Q_{ixo}. Including this and the temperature dependence due to self-heating, v_{xo} is modeled as [6]-[7]

$$v_{xo} = \frac{v_{inj}}{\left(1+\theta_v\frac{Q_{ixo}}{C_{inv}}\right)}(1 - \eta_v I_D V_D) \qquad (17)$$

where v_{inj} is the bias independent injection velocity at low channel charge. The term in the denominator accounts for carrier scattering and the last term in the numerator accounts for velocity reduction due to self-heating. θ_v and η_v are fitting parameters. Carrier mobility also decreases due to scattering and self-heating and is modeled as [5]-[6]

$$\mu = \frac{\mu_0}{\left(1+\theta_\mu\frac{Q_{ixo}}{C_{inv}}\right)\left(1+\frac{\eta_\mu I_D V_D}{T_o}\right)^{\varepsilon}} \qquad (18)$$

Here θ_μ, η_μ and ε are fitting parameters and T_o is reference temperature. The detailed procedure for the extraction of these parameters is provided at the end of this manual. The following lines in the Verilog-A file implement the core-equations of the transistor drain current described in this section.

Analog function: calc_iq

Function I/O definition

```
analog function real calc_iq;
output idsout,qgsout,qgdout,qcout,qbout,qsout;
input vgsin,vdsin,qcbflag,vcin,vbin,qgsflag,dirin,tambin,tnomin,phitin,w,lin,cgin,cs,cc,
cb,vto,ss;
input delta1,delta2,nd,alpha,vel0,mu0,beta,mtheta,vtheta;
```

Current formulation

```
absvdsin    = absfunc( vdsin );
vgdin       = vgsin - vdsin;
alpha_phit  = alpha * phitin;
n           = ss / ( `M_LN10 * phitin ) + nd * absvdsin;
vtof        = vto + vtzeta * ( tambin - tnomin );
if (dibsat != 0) begin
  vsatdibl  = absvdsin / ( pow(( 1.0 + pow( absvdsin / dibsat, beta)),( 1.0/beta )));
end else begin
  vsatdibl  = 0;
end
delta       = ( delta1 - vsatdibl * delta2 ) * absvdsin;
two_n_phit  = 2.0 * n * phitin;
qref        = cgin * two_n_phit;
// Qinvv
myarg       = vtof - delta - alpha_phit / 2.0;
exparg      = (( mmax( vgsin,vgdin ) - myarg ) / ( alpha_phit ));
if (exparg > `M_MAXEXP) begin
  ff        = 0.0;
end else if (exparg < -`M_MAXEXP) begin
  ff        = 1.0;
end else begin
  ff        = 1.0 / ( 1.0 + exp( exparg ));
end
eta         = ( mmax( vgsin,vgdin ) - ( vtof - delta - 0.1 * alpha_phit * ff )) / two_n_phit;
if (eta > `M_MAXEXP) begin
  qinvv     = qref * eta;
end else if (eta < -`M_MAXEXP) begin
  qinvv     = 0;
end else begin
  qinvv     = qref * ln( 1.0 + exp( eta ));
end
// velocity
muf         = mu0 / (( pow(( tambin / tnomin ), epsilon )) * ( 1.0 + mtheta * qinvv /cgin ));
vx          = vel0 * (( 1.0 + vzeta * tnomin ) / ( 1.0 + vzeta * tambin )) * ( 1.0 + lambda *
absvdsin /lin) / ( 1.0 + vtheta * qinvv/ cgin );
vxf         = 2.0 * ff * phitin * muf / lin + ( 1.0 - ff ) * vx;
vdsats      = vx * lin / muf;
vdsats1     = vdsats * sqrt( 1.0 + 2.0 * qinvv / cgin / vdsats ) - vdsats;
vdsat       = vdsats * ( 1.0 - ff ) + two_n_phit * ff;
vdsat1      = vdsats1 * ( 1.0 - ff ) + two_n_phit * ff;
fsd         = 1.0 / pow( 1.0 + pow( mmax( 0,( vdsin / vdsat1 )),beta ),1.0 / beta);
vdx         = vdsin * fsd;
fds         = 1.0 / pow( 1.0 + pow( mmax( 0,( -vdsin / vdsat1 )),beta),1.0 / beta);
vsx         = -vdsin * fds;
```

Source charge formulation

```
exparg      = ( vgsin - myarg ) / ( alpha_phit );
if (exparg > `M_MAXEXP) begin
  ffs      = 0.0;
end else if (exparg < -`M_MAXEXP) begin
  ffs      = 1.0;
end else begin
  ffs      = 1.0  /( 1.0 +  exp( exparg ));
end
etas       = ( vgdin - vsx - ( vtof - delta - 0.1 * alpha_phit * ffs )) / two_n_phit;
if (etas > `M_MAXEXP) begin
  qinvs    = qref * etas;
end else if (etas < -`M_MAXEXP) begin
  qinvs    = 0;
end else begin
  qinvs   = qref * ln( 1.0 + exp( etas ));
end
```

Drain charge formulation

```
exparg      = ( vgdin - myarg ) / ( alpha_phit );
if (exparg > `M_MAXEXP) begin
  ffd      = 0.0;
end else if (exparg < -`M_MAXEXP) begin
  ffd      = 1.0;
end else begin
  ffd      = 1.0 / ( 1.0 + exp( exparg ));
end
etad       = ( vgsin - vdx - ( vtof - delta - 0.1 * alpha_phit * ffd )) / two_n_phit;
if (etad > `M_MAXEXP) begin
  qinvd    = qref * etad;
end else if (etad < -`M_MAXEXP) begin
  qinvd    = 0;
end else begin
  qinvd    = qref * ln( 1.0 + exp( etad ));
end
```

Drain current formulation

```
vdsc       = ( qinvs - qinvd ) / cgin;
myarg      = vdsc / vdsat;
fsat       = myarg / ( pow( 1.0 + pow( absfunc( myarg ),beta), 1.0 / beta));
vel        = vxf * fsat;
idsout     = type * w * ngf * 0.5 * ( qinvs + qinvd ) * vel;
```

This completes the Verilog-A code for modeling drain current in GaN HEMTs. The model is fully symmetric with regard to S/D and satisfies the Gummel symmetry tests. In addition to currents, charges associated with the device are to be modeled to enable dynamic device applications. This is explained in the following section.

4. Transistor channel charge formulation

Any compact model in addition to models for terminal currents must also include model for terminal charges. Models for charges (and hence capacitances) are essential to reproduce dynamic behavior of devices for circuit simulation purposes. MVSG model has model for all terminal charges. In addition to gate-charge of intrinsic transistor, the charges associated with all FPs are modeled in distributed fashion based on internal node voltages. The gate charge in each transistor element is partitioned into gate-source charge (Q_{GSi}) and gate-

drain charge (Q_{GDi}) using the well known Ward-Dutton charge partitioning. A simple single moment partition method is used to get analytical closed form expressions for Q_{GSi} and Q_{GDi}.

$$Q_{GSi} = \int_{x=0}^{x=L_g} \left(1 - \frac{x}{L_g}\right) Q_{Gi}(\mathrm{x})\mathrm{dx} \qquad (19a)$$

$$Q_{GDi} = \int_{x=0}^{x=L_g} \left(\frac{x}{L_g}\right) Q_{Gi}(\mathrm{x})\mathrm{dx} \qquad (19b)$$

Here $Q_{Gi}(\mathrm{x})$ is the areal charge density at any point 'x' in the channel. $Q_{Gi}(\mathrm{x})$ and its dependence on bias depends on the mode of transport of carriers in the channel. The model for charge partitioning based on quasi-ballistic transport and NVsat formulation is described in detail in [8]. Here a fully continuous, derivable and fully symmetric charge partitioning model based on DD transport including pinch-off and velocity saturation effects will be discussed. The model satisfies the charge symmetry tests (McAndrew tests) akin to Gummel symmetry for currents. Firstly model for gate charge in longer channel GaN HEMTs where transport is drift-diffusion (DD) based, either in velocity saturation or mobility limited regime will be discussed followed by charges associated with field plates and cross-coupled charges and body-charges.

Gate charge in drift diffusion regime

To model gate charge in DD regime, approach adopted by Prof. Tsividis is closely followed with the derivation procedure for gate charge in this regime is similar to that found in the book written by Prof. Tsividis (section 6.4.2, chapter 6) [9] and is extended to include Nvsat regime. The source and drain partitioned charges are based on **Qinvs0** and **Qinvd0** terms used for current formulation (DIBL effect is removed from these terms to avoid negative capacitances) and is therefore self-consistent with transport. The details of the model are discussed in [X] and only brief description of the expressions are given here:

$$Q_{inv} = \frac{2}{3} W L_g \left[\frac{Q_{invs0}^2 + Q_{invd0}^2 + Q_{invs0}Q_{invd0}}{Q_{invs0} + Q_{invd0}}\right] \qquad (20)$$

$$Q_s = \frac{2}{15} W L_g \left[\frac{2Q_{invs0}^3 + 3Q_{invd0}^3 + 4Q_{invs0}^2 Q_{invd0} + +6Q_{invd0}^2 Q_{invs0}}{Q_{invs0}^2 + Q_{invd0}^2 + 2Q_{invs0}Q_{invd0}}\right] \qquad (21)$$

$$Q_d = Q_{inv} - Q_s \qquad (22)$$

These definitions of Q_s and Q_d bring in self-consistency with transport model. Since expressions for Q_{invs} and Q_{invd} remain the same as that in model for current and (28) is arrived at based on physics (please refer [8] for more details), charge model is self-consistent with current model.

Field plate charges

The channel charge of the FPs is partitioned to their corresponding source and drain internal nodes using the expressions (20)-(22) Q_{invs} and Q_{invd} corresponding to the FPs. This is done via the function call to **calc_iq** with the corresponding FP parameters. However in addition to the channel charges, cross-coupled charges are associated with each FP due to fringing fields. That is, for each FP connected to gate (source) there is a

capacitance associated with between drain and other terminal: source (gate). So when **flagfpx**=0 an additional C_{GDx} component is present and for **flagfpx**=1 an additional C_{SDx} component is present. This cross-coupled capacitance has V_T corresponding to that FP (**vtofpx**) and fringing capacitance per unit width (**ccfpx**) extractable from CV measurements in off state. A detailed extraction procedure of these parameters is given section. 6. Here the formulation equations are given in (23).

$$Q_{C,FPX} = CC_{FPX}\, Wn_{FPX}\, \varphi_t ln\left(1 + exp\frac{V_{G(s)diFPX} - (V_{T,FPX} - \alpha\varphi_t F_f)}{n_{FPX}\, \varphi_t}\right) \qquad (23)$$

The body capacitance associated with each FP is computed in the same way as in (23)

$$Q_{B,FPX} = CB_{FPX}\, Wn_{FPX}\, \varphi_t ln\left(1 + exp\frac{V_{BdiFPX} - (V_{T,FPX} - \alpha\varphi_t F_f)}{n_{FPX}\, \varphi_t}\right) \qquad (24)$$

Finally, the capacitance associated with the gate field plate extension on the source-side is computed using similar method (instead of adding additional transistors for ease of computation). The capacitance is implemented only if **flagfpxs=1**.

$$Q_{S,FPX} = CS_{FPX}\, Wn_{FPX}\, \varphi_t ln\left(1 + exp\frac{V_{GsiFPX} - (V_{T,FPX} - \alpha\varphi_t F_f)}{n_{FPX}\, \varphi_t}\right) \qquad (25)$$

The following lines in the Verilog-A file implement the core-equations of the charge model described above.

Charge formulation

Source and drain charge formulation with DIBL removed

```
n0         = ss / ( `M_LN10 * phitin );
two_n_phit0  = 2.0 * n0 * phitin;
qref0       = cgin * two_n_phit0;
// Qinvv0
myarg0      = vtof - alpha_phit / 2.0;
exparg0     = (( mmax( vgsin,vgdin ) - myarg0 )/( alpha_phit ));
if (exparg0 > `M_MAXEXP) begin
  ff0      = 0.0;
end else if (exparg0 < -`M_MAXEXP) begin
  ff0      = 1.0;
end else begin
  ff0      = 1.0 / ( 1.0 + exp( exparg0 ));
end
eta0        = ( mmax( vgsin,vgdin ) - ( vtof - 0.1 * alpha_phit * ff0 )) / two_n_phit0;
if (eta0 > `M_MAXEXP) begin
  qinvv0    = qref0 * eta0;
end else if (eta0 < -`M_MAXEXP) begin
  qinvv0    = 0;
end else begin
  qinvv0  = qref0 * ln( 1.0 + exp( eta0 ));
end
muf0        = mu0 / (( pow(( tambin / tnomin ),epsilon )));
vx0         = vel0 * (( 1.0 + vzeta * tnomin ) / ( 1.0 + vzeta * tambin ));
```

```
vdsats0     = vx0 * lin / muf0;
vdsats10    = vdsats0 * sqrt( 1.0 + 2.0 * qinvv0 / cgin / vdsats0 ) - vdsats0;
vdsat10     = vdsats10 * ( 1.0 - ff0 ) + two_n_phit0 * ff0;
fsd0        = 1.0 / pow( 1.0 + pow( mmax(0,( vdsin / vdsat10 )),beta ),1.0 / beta);
vdx0        = vdsin * fsd0;
fds0        = 1.0 / pow( 1.0 + pow( mmax(0,( -vdsin / vdsat10 )),beta ),1.0 / beta);
vsx0        = -vdsin * fds0;
exparg0     = ( vgsin - myarg0 ) / ( alpha_phit );
if (exparg0 > `M_MAXEXP) begin
  ffs0      = 0.0;
end else if (exparg0 < -`M_MAXEXP) begin
  ffs0      = 1.0;
end else begin
  ffs0      = 1.0 / ( 1.0 + exp( exparg0 ));
end
etas0       = ( vgdin - vsx0 - ( vtof - 0.1 * alpha_phit * ffs0 )) / two_n_phit0;
if (etas0 > `M_MAXEXP) begin
  qinvs0    = qref0 * etas0;
end else if (etas0 < -`M_MAXEXP) begin
  qinvs0    = 0;
end else begin
  qinvs0  = qref0 * ln( 1.0 + exp( etas0 ));
end
exparg0     = ( vgdin - myarg0 ) / ( alpha_phit );
if (exparg0 > `M_MAXEXP) begin
  ffd0      = 0.0;
end else if (exparg0 < -`M_MAXEXP) begin
  ffd0      = 1.0;
end else begin
  ffd0    = 1.0 / ( 1.0 + exp( exparg0 ));
end
etad0       = ( vgsin - vdx0 - ( vtof - 0.1 * alpha_phit * ffd0 )) / two_n_phit0;
if (etad0 > `M_MAXEXP) begin
  qinvd0    = qref0 * etad0;
end else if (etad0 < -`M_MAXEXP) begin
  qinvd0    = 0;
end else begin
  qinvd0  = qref0 * ln( 1.0 + exp( etad0 ));
end
```

DD-channel charge partitioning

```
qs2         = qinvs0 * qinvs0 + 1e-38;
qs3         = qs2 * qinvs0 + 1e-57;
qd2         = qinvd0 * qinvd0 + 1e-38;
qd3         = qd2 * qinvd0 + 1e-57;
qsqd        = qinvs0 * qinvd0 + 1e-38;
qinvdd      = 2.0 / 3.0 * ( qs2 + qd2 + qsqd ) / ( qinvs0 + qinvd0 + 2e-19 );
qd1         = 2.0 * ( 2.0 * qs3 + 3.0 * qd3 + 4.0 * qs2 * qinvd0 + 6.0 * qd2 * qinvs0 ) / ( 15.0
* ( qs2+ qd2 + 2 * qsqd ));
qs          = qinvdd - qd1;
qd          = qd1;
qgsout      = w * ngf * lin * type * qs;
qgdout      = w * ngf * lin * type * qd;
```

FP cross-coupled and body charge formulation

```
if (qcbflag==1) begin
  etac     = ( vcin - ( vtof - 0.5 * alpha_phit )) / two_n_phit0;
  if (etac > `M_MAXEXP) begin
    exparg = etac;
  end else if (etac < -`M_MAXEXP) begin
    exparg = 0;
  end else begin
    exparg = ln( 1.0 + exp( etac ));
  end
  qcout    = w * ngf * type * cc * two_n_phit0 * exparg;
  etab     = ( vbin - ( vtof - 0.5 * alpha_phit )) / two_n_phit0;
  if (etab > `M_MAXEXP) begin
    exparg = etab;
  end else if (etab < -`M_MAXEXP) begin
    exparg = 0;
  end else begin
    exparg = ln( 1.0 + exp( etab )); end
  qbout    = w * ngf * type * cb * two_n_phit0 * exparg;
end else begin
  qcout    = 0;
  qbout    = 0;
end
```

FP source side charge formulation

```
  if (qgsflag==1) begin
  etags    = ( vgsin - ( vtof - 0.5 * alpha_phit )) / two_n_phit0;
  if (etags > `M_MAXEXP) begin
    exparg = etags;
  end else if (etags < -`M_MAXEXP) begin
    exparg = 0;
  end else begin
    exparg = ln( 1.0 + exp( etags  ));
  end
  qsout    = w * ngf * type * cs * two_n_phit0 * exparg;
end else begin
  qsout    = 0;
end
```

Model for fringing field capacitances

The constant metal-metal capacitance between two of the 4 terminals is calculated using parameters extracted from the capacitance vs. drain voltage measurements in off-state. The following lines of code execute these capacitances:

```
qofs          = w * ngf * cofsm * V(gi,s);
I(gi,s)       <+ ddt(qofs);
qofd          = w * ngf * cofdm * V(gi,d);
I(gi,d)       <+ ddt(qofd);
qofds         = w * ngf * cofdsm * V(d,s);
I(d,s)        <+ ddt(qofds);
qofdsub       = w * ngf * cofdsubm * V(d,b);
I(d,b)        <+ ddt(qofdsub);
qofssub       = w * ngf * cofssubm * V(s,b);
I(s,b)        <+ ddt(qofssub);
qofgsub       = w * ngf * cofgsubm * V(gi,b);
I(gi,b)       <+ ddt(qofgsub);
```

5. Gate current formulation

Gate current formulation for Schottky gated GaN HEMTs (typically in RF-GaN HEMTs) includes two Schottky diodes between gate-source and gate-drain terminals. The model is identical for the two diodes but the parameters can be independently set. The forward diode current is given by the expression

$$I_{Gsi(di)} = Wn_{gf}\, i_{js(d)} \left(\frac{T}{T_0}\right)^{egate} exp\frac{-P_{Gparam1}V_{jG}}{\varphi_t}\left(exp\frac{P_{Gs(d)}V_{Gsi(di)}}{\varphi_t} - 1\right) \qquad (26)$$

which includes the temperature dependence of the reverse saturation current, bandgap dependence (through V_{jG}) and ideality factor dependence through $P_{Gs(d)}$ and accounts for changing ideality factor under high-injection conditions.

$$P_{Gs(d)} = P_{Gparams(d)}((1 - fracs(d))F_{f,gate} + fracs(d)) \qquad (27)$$

with $F_{f,gate}$ having similar definition as in (7) and fracs(d) parameter determines the fractional change in the ideality factor from its low injection value of $P_{Gparams(d)}$. In addition to forward current, the reverse GIDL and recombination currents are captured through empirical diode equations to account for drain voltage dependence on reverse-leakage gate currents.

$$I_{Grecsi(di)} = Wn_{gf}\, i_{recs(d)} \left(\frac{T}{T_0}\right)^{egate} \left(exp\frac{P_{Grecs(d)}F_{recs(d)}}{\varphi_t} - 1\right) \qquad (28)$$

$$F_{recs(d)} = \frac{-V_{Gsi(di)}}{\left(1+\left(\frac{V_{Gsi(di)}}{V_{Gsatqs(d)}}\right)^{betarec}\right)^{1/betarec}} \qquad (29)$$

The following lines in the Verilog-A file implement the core-equations of the gate-current model described above.

Analog function: calc_ig

Function I/O definition

```
analog function real calc_ig;
output igout;
input vgin, phitin;
input vgsatin, alphagin, fracin, pg_paramin, pbdgin, vbdgin, tambin, tnomin;
input w, ngf,ijin, kbdgatein, vgsatqin, betarecin, irecin, pgsrecin, pg_param1, vjg;
real igout, vgin, phitin, vgsatin, alphagin, fracin, pg_paramin, pbdgin, vbdgin, tambin;
real w, ngf,ijin, kbdgatein, vgsatqin, betarecin, irecin, pgsrecin, pg_param1, vjg;
real  alpha_phit, t0, ffvgin, pgin, iginbd, tfacdiode, igindiode, tnomin, frecgin, iginrec;
```

Current formulation

```
alpha_phit   = alphagin * phitin;
expphib      = pg_param1 / phitin * (- vjg);
t0           = explim( expphib );
expffvarg    = ( vgin - ( vgsatin - alphagin * alpha_phit / 2.0))/( alphagin * alpha_phit );
if (expffvarg > `M_MAXEXP) begin
    ffvgin = 0.0;
end else if (expffvarg < -`M_MAXEXP) begin
    ffvgin = 1.0;
end else begin
    ffvgin  = 1.0 / ( 1.0 + exp( expffvarg )); end
```

```
pgin       = ( fracin * pg_paramin + ( 1.0 - fracin) * pg_paramin * ffvgin );
expbdarg1  = pbdgin * ( -vgin  - vbdgin ) + expphib;
expbdarg2  = -pbdgin * vbdgin + expphib;
expbd1     = explim( expbdarg1 );
expbd2     = explim( expbdarg2 );
iginbd     = ( expbd1 - expbd2 );
tfacdiode  = pow( ( tambin / tnomin ) , 3.0 );
isdiodeout = w * ngf * ijin * tfacdiode;
expiforarg = pgin / phitin * vgin + expphib;
expifor    = explim( expiforarg );
igindiode  = isdiodeout * ( expifor - ( kbdgatein * iginbd ) - t0 );
frecgin    = -vgin / pow(( 1.0 + pow( absfunc( vgin  / vgsatqin ), betarecin )), 1.0 /
betarecin );
isrecout   = -w * ngf * irecin * tfacdiode * 1.0;
expirevarg = pgsrecin / phitin * frecgin;
expirev    = explim( expirevarg );
iginrec    = isrecout * ( expirev - 1.0 );
igout      = igindiode + iginrec;
calc_ig    = igout;
```

Gate-resistance formulation

```
if (rg <= minr) begin
  V(g,gi)      <+ 0;
end else begin
  I(g,gi)      <+ V(g,gi) / rg;
end
```

6. Charge trapping effects

The dynamic current collapse effect in GaN HEMTs resulting in higher knee voltage, lower on-currents under switching conditions is well known [2]. The knee-walk out effect is accounted for in MVSG by increasing the sheet resistance/threshold voltage of drain-side access region dynamically through a trap-time constant. A single RC trap time constant is chosen for fitting frequency dependence in Toshiba data as trapping and de-trapping time constants cannot be separated from available industry. Two time constants for charging and discharging of traps can be included in MVSG model if required in subsequent release.

$$V_{tcollapse0} = trapfac * (alpha1\, V_{DG} + alpha3\left(exp\frac{V_{DG}-\text{vttrap}}{alphat2}\right)) \qquad (30)$$

This is the source function for charge trapping which has the requisite bias and temperature dependence. Beyond vttrap, the trapping effect is exponential as seen from Toshiba data. This is fed into the RC network with time constant (taut). The resulting $V_{tcollapse}$ function from the RC network is fed to the sheet resistance (Rsh) of the drain access region which increases the knee-voltage and lowers the on-currents only under switching conditions when $V_{tcollapse}$ is non-zero.

Charge trapping module

```
if ( trapselect  != 0) begin
  vtcollapse0   = alphat1 * abs(V(d) - V(g)) + limexp( (V(d) - V(g) - vttrap) / alphat2 );
  vtcollapse    = V(tr);
  I(tr)         <+ -vtcollapse0 + ddt(taut * V(tr));
  I(tr)         <+ V(tr);
  drsht         = 1.0 + (vtcollapse) * ttrapfac;
end else begin
  vtcollapse0   = 0; vtcollapse    = 0; V(tr)       <+ 0; drsht       = 1.0; end
```

MVSG Model: Parameter list

The following table shows the list of all parameters needed for fitting MVSG model to experimental data. The description and data type of the parameters are also listed. The model for CMC was benchmarked against Toshiba 1μm gate-length HV-GaN HEMTs and Qorvo 250 nm gate-length RF-GaN HEMTs. These were released along with the default parameters in the master Verilog-A files in P-3 with the file names: **mvsg_toshiba.va and mvsg_qorvo.va.** In P-4 we use the default parameter set in the model which were extracted for devices used at MIT.

Toshiba parameters: paramsHV.txt

Parameter	Default Value	Units	Description
w	3e-3	m	Width per Finger
l	1.0e-6	m	Length
ngf	1.0		Number of Fingers
version	1.00		Version
tnom	27.0	degC	Nominal temperature for model
type	1		nFET=1 pFET=-1
cg	1.70e-03	F/m^2	Gate Cap/Area
Metal capacitances			
cofsm	1.6e-9	F/m	Gate - Source Outer Fringing Cap/Width
cofdm	1.0e-19	F/m	Gate - Drain Outer Fringing Cap/Width
cofdsm	8.0e-10	F/m	Source - Drain Outer Fringing Cap/Width
cofdsubm	0.0e-14	F/m	Sub - Drain Outer Fringing Cap/Width
cofssubm	0.0e-14	F/m	Sub - Source Outer Fringing Cap/Width
cofgsubm	3e-10	F/m	Sub - Gate Outer Fringing Cap/Width
Intrinsic transistor transport and electrostatic parameters			
rsh	100.0	Ohms/Sq	2-DEG Sheet Resistance
rcs	0.21e-2	Ohms*m	Source contact resistance * Width
rcd	0.21e-2	Ohms*m	Drain contact resistance * Width
vx0	1.2e5	m/s	Source injection velocity
mu0	0.100	m^2/Vs	Low-field Mobility
beta	1.16	m/s	Linear to Saturation Parameter
vto	-3.9	V	Threshold Voltage
ss	0.10	V/dec	Sub-threshold Slope
delta1	0.005		DIBL Coefficient
delta2	0.00		DIBL Coefficient
dibsat	10.0	V	DIBL Saturation Voltage
nd	0.0		Punchthrough factor for Subth Slope
alpha	3.5		Weak to Strong Inversion Factor
lambda	0.0	1/V	CLM Parameter
vtheta	0.0		Velocity reduction parameter with Vg
mtheta	0.0		Mobility reduction parameter with Vg
vzeta	4e-3		VXO dependence on temperature
vtzeta	-1e-3		vto dependence on temperature
epsilon	3.0		Mobility dependence on temperature
rct1	0.0	Ohm/K	Rsh and Rc temperature coefficient
rct2	0.0	Ohm/K^2	Rsh and Rc temperature coefficient

Source access region implicit-gate transistor parameters

lgs	2.0e-6	m	Source access region distance
vtors	-650	V	SAR Threshold Voltage
cgrs	80e-5	F/m^2	SAR to Drain Cap/Area
vx0rs	1.0e5	m/s	SAR Source injection velocity
mu0rs	0.100	m^2/Vs	SAR Low-field Mobility
betars	1.1		Linear to Saturation Parameter
delta1rs	4e-4		SAR DIBL Coefficient
srs	0.065	V/dec	SAR Sub-threshold Slope
ndrs	0.0		SAR Punchthrough factor for Subth Slope
vthetars	0.0		Velocity reduction parameter with Vg
mthetars	0.0		Mobility reduction parameter with Vg
alphars	3.5		SAR Weak to Strong Inversion Factor

Drain access region implicit-gate transistor parameter

lgd	7.0 e-6	m	Drain access region distance
vtord	-650.0	V	DAR Threshold Voltage
cgrd	70e-5	F/m^2	DAR to Drain Cap/Area
vx0rd	1.0e5	m/s	DAR Source injection velocity
mu0rd	0.100	m^2/Vs	DAR Low-field Mobility
betard	1.1		Linear to Saturation Parameter
delta1rd	4e-4		DAR DIBL Coefficient
srd	0.08	V/dec	DAR Sub-threshold Slope
ndrd	0.0		DAR Punchthrough factor for Subth Slope
vthetard	0.0		Velocity reduction parameter with Vg
mthetard	0.0		Mobility reduction parameter with Vg
alphard	3.5		DAR Weak to Strong Inversion Factor

FP1 transistor parameter

flagfp1	1		Flag parameter: GFP=1 or SFP=0
lgfp1	3.5e-6	m	FP Length
vtofp1	-44.5	V	FP Threshold Voltage
cgfp1	2.0e-4	F/m^2	FP to Drain Cap/Area
flagfp1s	1		cfp1s select=1 or cfp1s not select=0
cfp1s	1e-19	F/m	FP (source-side) to Source Cap/Width
ccfp1	0.9e-10	F/m	Source or Gate to Drain Cap/Width
cbfp1	0.0	F/m	Body to Drain Cap/Width
vx0fp1	1.2e5	m/s	FP Source injection velocity
mu0fp1	0.2	m^2/Vs	FP Low-field Mobility
betafp1	1.16		Linear to Saturation Parameter
delta1fp1	0.00		FP DIBL Coefficient
sfp1	3.2	V/dec	FP Sub-threshold Slope
ndfp1	0.0		FP Punchthrough factor for Subth Slope
vthetafp1	0.0		Velocity reduction parameter with Vg
mthetafp1	0.0		Mobility reduction parameter with Vg
alphafp1	1e-2		FP Weak to Strong Inversion Factor

FP2 transistor parameter

flagfp2	0		Flag parameter: GFP=1 or SFP=0
lgfp2	3.5e-6	m	FP Length
vtofp2	-60.0	V	FP Threshold Voltage
cgfp2	9.0e-5	F/m^2	FP to Drain Cap/Area
flagfp2s	0		cfp2s select=1 or cfp2s not select=0
cfp2s	0.0	F/m	FP (source-side) to Source Cap/Width

ccfp2	0.65e-10	F/m	Source or Gate to Drain Cap/Width
cbfp2	0.0	F/m	Body to Drain Cap/Width
vx0fp2	1.9e5	m/s	FP Source injection velocity
mu0fp2	0.29	m^2/Vs	FP Low-field Mobility
betafp2	1.16		Linear to Saturation Parameter
delta1fp2	0.00		FP DIBL Coefficient
sfp2	4.1	V/dec	FP Sub-threshold Slope
ndfp2	0.0		FP Punchthrough factor for Subth Slope
vthetafp2	0.0		Velocity reduction parameter with Vg
mthetafp2	0.0		Mobility reduction parameter with Vg
alphafp2	1.3e3		FP Weak to Strong Inversion Factor
rgsp	0.0	Ohms*m	Gate resistance * Width
rth	125	K/W	Thermal resistance
cth	1e-4	s.W/K	Thermal capacitance

Charge trapping model

trapselect	0		Select knob for charge trapping
vttrap	230	V	Trapping stress time constant
taut	3.0e-5	s	Trap time constant
alphat1	1e-4		Trap coefficient on bias stress
alphat2	21		Trap coefficient on bias stress
tempt	1e-4		Temperature coefficient for trapping

Qorvo parameters: paramsRF.txt

Parameter	Default Value	Units	Description
w	90e-6	m	Width per Finger
l	0.15e-6	m	Length
ngf	10.0		Number of Fingers
version	1.00		Version
tnom	27.0	degC	Nominal temperature for model
type	1		nFET=1 pFET=-1
cg	6.30e-03	F/m^2	Gate Cap/Area

Metal capacitances

cofsm	650e-12	F/m	Gate - Source Outer Fringing Cap/Width
cofdm	0	F/m	Gate - Drain Outer Fringing Cap/Width
cofdsm	0	F/m	Source - Drain Outer Fringing Cap/Width
cofdsubm	0	F/m	Sub - Drain Outer Fringing Cap/Width
cofssubm	0	F/m	Sub - Source Outer Fringing Cap/Width
cofgsubm	0 s	F/m	Sub - Gate Outer Fringing Cap/Width

Intrinsic transistor transport and electrostatic parameters

rsh	150.0	Ohms/Sq	2-DEG Sheet Resistance
rcs	1e-4	Ohms*m	Source contact resistance * Width
rcd	1e-4	Ohms*m	Drain contact resistance * Width
vx0	1.0e5	m/s	Source injection velocity
mu0	0.140	m^2/Vs	Low-field Mobility
beta	2.0	m/s	Linear to Saturation Parameter
vto	-2.5	V	Threshold Voltage
ss	0.39	V/dec	Sub-threshold Slope
delta1	80e-3		DIBL Coefficient
delta2	0.00		DIBL Coefficient
dibsat	4.0	V	DIBL Saturation Voltage
nd	0.2		Punchthrough factor for Subth Slope

alpha	10		Weak to Strong Inversion Factor
lambda	0.0	1/V	CLM Parameter
vtheta	0.0		Velocity reduction parameter with Vg
mtheta	0.0		Mobility reduction parameter with Vg
vzeta	1e-3		VXO dependence on temperature
vtzeta	-4e-4		vto dependence on temperature
epsilon	0.083		Mobility dependence on temperature
rct1	0.0	Ohm/K	Rsh and Rc temperature coefficient
rct2	0.0	Ohm/K^2	Rsh and Rc temperature coefficient

Source access region implicit-gate transistor parameters

lgs	1.0e-6	m	Source access region distance
vtors	-650	V	SAR Threshold Voltage
cgrs	45e-5	F/m^2	SAR to Drain Cap/Area
vx0rs	1.0e5	m/s	SAR Source injection velocity
mu0rs	0.100	m^2/Vs	SAR Low-field Mobility
betars	1.0		Linear to Saturation Parameter
delta1rs	0.1		SAR DIBL Coefficient
srs	0.065	V/dec	SAR Sub-threshold Slope
ndrs	0.0		SAR Punchthrough factor for Subth Slope
vthetars	0.0		Velocity reduction parameter with Vg
mthetars	0.0		Mobility reduction parameter with Vg
alphars	40		SAR Weak to Strong Inversion Factor

Drain access region implicit-gate transistor parameter

lgd	1.6 e-6	m	Drain access region distance
vtord	-650.0	V	DAR Threshold Voltage
cgrd	8.00e-3	F/m^2	DAR to Drain Cap/Area
vx0rd	1.0e5	m/s	DAR Source injection velocity
mu0rd	0.100	m^2/Vs	DAR Low-field Mobility
betard	1.3		Linear to Saturation Parameter
delta1rd	0.2		DAR DIBL Coefficient
srd	1.8	V/dec	DAR Sub-threshold Slope
ndrd	3.8		DAR Punchthrough factor for Subth Slope
vthetard	0.0		Velocity reduction parameter with Vg
mthetard	0.0		Mobility reduction parameter with Vg
alphard	40		DAR Weak to Strong Inversion Factor
rgsp	0.0	Ohms*m	Gate resistance * Width
rth	2	K/W	Thermal resistance
cth	1e-4	s.W/K	Thermal capacitance

Gate current model

igmod	1		Choice of gate leakage model set to 0
vjg	5	V	Gate diode cut in voltage [V]
pg_param1	0.5	1/V	Something like 1/eta
pg_params	0.5	1/V	G-S something like 1/eta*Vt
ijs	1.0	A/m	G-S reverse leakage current normalized to width [A/cm]
vgsats	3	V	G-S high injection effect
fracs	1		G-S fractional change in ideality factor due to high injection
alphags	10		G-S high injection smoothing parameter
pg_paramd	0.5	1/V	G-D something like 1/eta*Vt [1/V]

ijd	1.0	A/m	G-D reverse leakage current normalized to width [A/cm]
vgsatd	3	V	G-D high injection effect
fracd	1		G-D fractional change in ideality factor due to high injection
alphagd	10		G-D high injection smoothing parameter
pgsrecs	0.5		G-S something like 1/eta
irecs	1.0e-18	A/m	G-S reverse leakage current normalized to width [A/cm]
vgsatqs	5	V	G-S mimics depletion saturation
vbdgs	600	V	G-S soft breakdown voltage of GD diode
pbdgs	4		G-S fitting parameter
kbdgates	0.0		G-S fitting parameter
betarecs	0.5		G-S fitting parameter
pgsrecd	0.5		G-D something like 1/eta
irecd	1.0e-18	A/m	G-D reverse leakage current normalized to width [A/cm]
vgsatqd	5	V	G-D mimics depletion saturation
vbdgd	600	V	G-D soft breakdown voltage of GS diode
pbdgd	4		G-D fitting parameter
kbdgated	0.0		G-D fitting parameter
betarecd	0.5		G-D fitting parameter

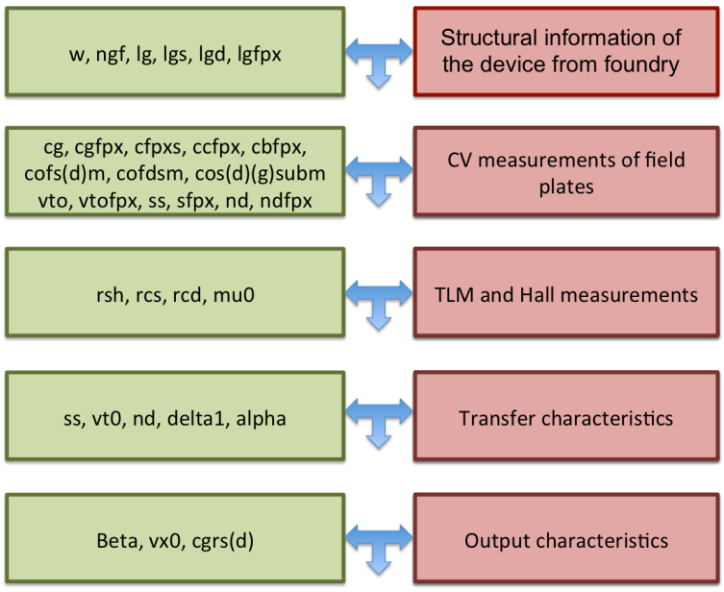
The default parameter set used with the QAsuite in P-4 release can be found in the **parameters** folder under the name: **dmodeParameters.txt** and are listed here.

+ tnom	27	+ lgd	4.85E-06	+ ndfp2	0	+ pg_params	1
+ cg	0.004	+ vtord	-650	+ vthetafp2	0	+ ijs	1E-12
+ cofsm	1E-09	+ cgrd	0.0043	+ mthetafp2	0	+ vgsats	1
+ cofdm	1E-10	+ vx0rd	100000	+ alphafp2	0.01	+ fracs	0.5
+ cofdsm	1E-10	+ mu0rd	0.1	+ flagfp3	0	+ alphags	10
+ cofdsubm	0	+ betard	1	+ lgfp3	0	+ pg_paramd	1
+ cofssubm	0	+ delta1rd	0.35	+ vtofp3	-90	+ ijd	1E-12
+ cofgsubm	0	+ srd	0.3	+ cgfp3	0.00009	+ vgsatd	1
+ rsh	150	+ ndrd	3.8	+ flagfp3s	1	+ fracd	0.5
+ rcs	0.0008	+ vthetard	0	+ cfp3s	1E-19	+ alphagd	10
+ rcd	0.0008	+ mthetard	0	+ ccfp3	9E-11	+ pgsrecs	0.5
+ vx0	300000	+ alphard	3.5	+ cbfp3	0	+ irecs	1E-18
+ mu0	0.135	+ flagfp1	1	+ vx0fp3	120000	+ vgsatqs	2
+ beta	1.5	+ lgfp1	0	+ mu0fp3	0.2	+ vbdgs	600
+ vto	-2.72	+ vtofp1	-44.5	+ betafp3	1	+ pbdgs	4
+ ss	0.12	+ cgfp1	0.0002	+ delta1fp3	0	+ betarecs	2
+ delta1	0.016	+ flagfp1s	1	+ sfp3	3.2	+ kbdgates	0
+ delta2	0	+ cfp1s	1E-19	+ ndfp3	0	+ pgsrecd	0.8
+ dibsat	10	+ ccfp1	9E-11	+ vthetafp3	0	+ irecd	0.00002
+ nd	0	+ cbfp1	0	+ mthetafp3	0	+ vgsatqd	0.8
+ alpha	3.5	+ vx0fp1	120000	+ alphafp3	0.01	+ vbdgd	600
+ lambda	0	+ mu0fp1	0.2	+ flagfp4	0	+ pbdgd	4

+ vtheta	0	+ betafp1	1	+ lgfp4	0	+ betarecd	0.25
+ mtheta	0	+ delta1fp1	0	+ vtofp4	-110	+ kbdgated	0
+ vzeta	150000	+ sfp1	3.2	+ cgfp4	0.00006	+ rth	25
+ vtzeta	-0.0004	+ ndfp1	0	+ flagfp4s	1	+ cth	0.0001
+ epsilon	2.3	+ vthetafp1	0	+ cfp4s	1E-19	+ gmdisp	0
+ rct1	0	+ mthetafp1	0	+ ccfp4	9E-11	+ taugmrf	0.0001
+ rct2	0	+ alphafp1	0.01	+ cbfp4	0	+ trapselect	0
+ flagres	0	+ flagfp2	0	+ vx0fp4	120000	+ ctrap	0.001
+ lgs	0.000003	+ lgfp2	0	+ mu0fp4	0.2	+ vttrap	230
+ vtors	-650	+ vtofp2	-74.5	+ betafp4	1	+ taut	0.00003
+ cgrs	0.005	+ cgfp2	0.0001	+ delta1fp4	0	+ alphat1	0.0001
+ vx0rs	100e3	+ flagfp2s	1	+ sfp4	3.2	+ alphat2	21
+ mu0rs	0.1	+ cfp2s	1E-19	+ ndfp4	0	+ tempt	0.0001
+ betars	1	+ ccfp2	9E-11	+ vthetafp4	0	+ noisemod	0
+ delta1rs	0.1	+ cbfp2	0	+ mthetafp4	0	+ shs	2
+ srs	0.1	+ vx0fp2	120000	+ alphafp4	0.01	+ shd	2
+ ndrs	0	+ mu0fp2	0.2	+ igmod	1	+ kf	0.001
+ vthetars	0	+ betafp2	1	+ rgsp	0	+ af	1
+ mthetars	0	+ delta1fp2	0	+ vjg	1.1	+ ffe	1
+ alphars	3.5	+ sfp2	3.2	+ pg_param1	0.82		

Parameter extraction procedure for MVSG Model

The following flowchart shows the sequence of extraction procedure of important parameters of MVSG model.



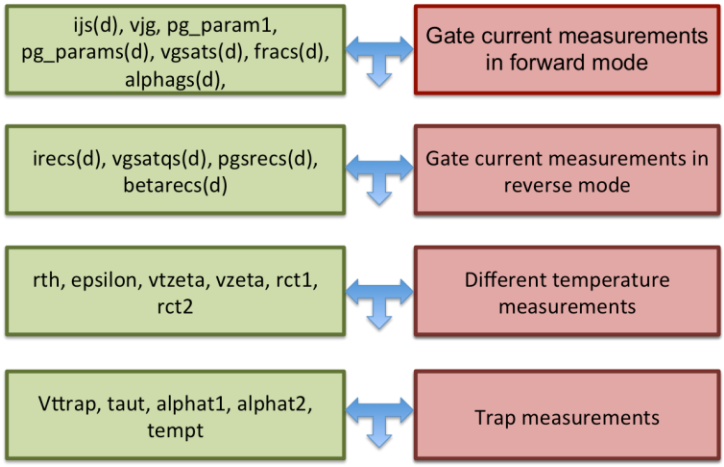


Fig. 7: Flowchart showing parameter extraction flow. This is not the exhaustive list of parameters but the most significant ones. Most of the other parameters are either fitting parameters or constants for GaN HEMT. All parameters will be discussed.

Device parameters

Geometry and structural information are best provided by foundry. For the model, geometry parameters needed are: Gate length (L_g), Source access region (L_{gs}), drain-access region length (L_{gd}), device-width (W). In addition, parameters related to field plate such as field plate length (L_{gfpx}), inter-layer dielectric thickness etc. will be necessary for modeling. Other additional useful parameters required by the model are: Low field mobility (μ_o), Contact resistance (R_c) and sheet resistance (R_{sh}), 2DEG density. If these are not provided, additional measurements might be needed to extract them. μ_o and R_{sh} extraction would require Hall measurements and special hall structures. R_c can be extracted by measuring resistances of TLM structures of different lengths and extracting the offset at L_g=0. Correct extraction of these parameters can also be verified from R_{on} match in output characteristics.

C_g extraction

C_g is an important model parameter in MVSG model. Its accurate extraction is essential for correct modeling. C_g must be extracted from CV measurements rather than from analytical calculation. Accurate analytical calculation must also include quantum correction as charge centroid in 2DEG is shifted away from the interface. This needs dedicated calculations/simulation, which from a compact modeling perspective might not be critical as long as we can directly measure the capacitance. To get C_g, two terminal CV (with V_{DS}=0) of devices with different gate length but identical widths and access region lengths must be measured. The gate to channel capacitance in strong accumulation scales as a function of L_g. From the slope we get the value of C_g (areal gate capacitance) and the intercept gives the parasitic capacitance. Parasitic capacitance includes outer fringing capacitance (C_{of}) and pad parasitic. To remove the pad parasitic, we need CV of open test structures.

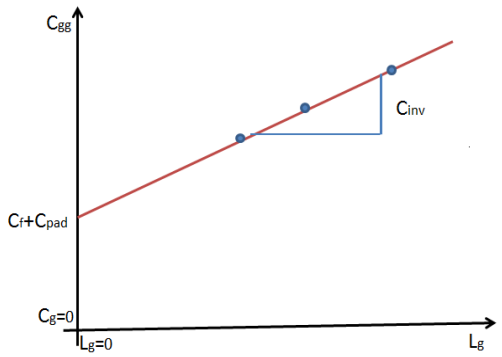


Fig. 8: Illustration of extraction of C_g devices of different gate lengths

Device parameters for FPs

Geometry and structural information of field plates along with their configuration are best provided by foundry. For the FP model, the only geometry parameter needed is gate length of FPs (L_{gfpx}). It is the length of the FP metal, which has direct control over the 2DEG under it. So if a SFP metal runs from the source contact over the intrinsic-gate metal and gate FP metal, the SFP gate length is only that length of the SFP metal that extends beyond the edge of the GFP metal to its edge (where there is no other metal between it and the 2DEG).

Extraction of parameters from C_{iss} vs. V_g measurements

Gate capacitance measurements vs. V_G at V_{DS}=0V will yield the areal gate capacitances and V_Ts of all gate-connected field plates. This is shown in Fig. 8 where at V_G=**vto** of the FET can be obtained and the step in CV curve at this V_G normalized to the width and gate-length (which are known) gives **cg** the areal gate-capacitance. Similarly the transition at V_G=-50V the figure is due to the depletion of the GFP1 occurring at its V_T (**vtofp1**) and the areal gate-capacitance (**cgfp1**) is the step in the CV curve at that VG. In addition, the electrostatic parameters such as sub-threshold slope **sfp1** can be obtained from the slope of transition. The off-state capacitance obtained from calibrated CV measurements yields the total metal capacitances associated with gate terminal (**cofsm+cofdm**). Individual components can then be obtained from Cgs and Cgd measurements using bias-Ts to apply the DC bias.

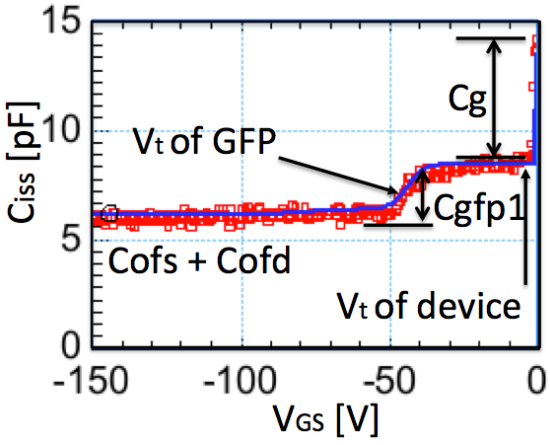


Fig.9: Illustration of extraction of gate-field plate parameters of devices from C_{iss} vs. Vg measurements

Extraction of parameters from C_{oss}, C_{rss}, C_{iss} vs. V_d measurements

Input, output and reverse transfer capacitance measurements vs. V_D in off-state will yield the areal gate capacitances, cross-coupled capacitances and V_Ts of all field plate transistors. Fig. 9 shows representative C_{iss}, C_{oss} and C_{rss} plots which shows transitions at V_D=V_Ts of different field plates which are due to depletion of these transistors. From C_{iss} (or C_{rss}) the areal gate capacitances of GFP transistors (**cgfp1**) (can be cross-checked from previous plot) and cross-coupled capacitances of SFP transistors (**ccfp2**) can be obtained. Metal capacitances between gate- and other terminals (**cofs, cofd, cofgsub**) of the device can be extracted as well. From C_{oss} plot, the capacitances associated with the source terminal can be obtained, which includes the areal-gate capacitances of SFP transistors (**cgfp2**) and cross-coupled capacitances of GFP transistors (**ccfp1**) along with the metal capacitances associated with source-drain terminals (**cofds**).

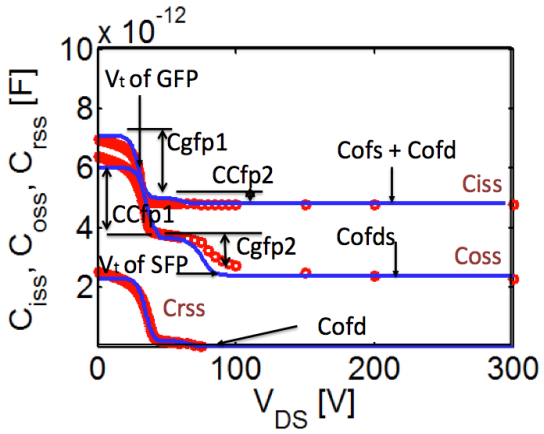


Fig.10: Illustration of extraction of field plate parameters of devices from capacitance vs. drain voltage measurements

This completes the important parameter extraction flow for the field plates of GaN HEMT. The transport parameters associated with the field plates should be kept the same as those extracted from the IV characteristics for the intrinsic transistor, unless model fits demand that they be set different. However usually parameters such as mobility, carrier velocity do not change for different transistors in the model sub-circuit. Stand-alone FP transistors or test-structures with devices having the FP connections whose gate-bias can be independently controlled can used to get a more accurate estimate of electrostatic and transport parameters of FPs.

Extraction of V_{to}, S and DIBL (delta1)

Threshold voltage (V_t) computation requires knowledge of piezoelectric charges at the interface, heterostructure composition and thickness. Again the model is simplistic in the sense that V_{to} needed for the model can be extracted from device data. The requirement is one data point (V_G, I_D, V_D) in weak accumulation (just beyond strong to weak accumulation transition) at low V_D (~0V where DIBL has negligible impact). Alternately V_{to} can be approximated as V_G at the same (V_G, I_D, V_D) point on transfer curve.

Sub threshold slope (S) is obtained from the slope of the transfer curve on log scale in weak accumulation regime. Low V_D is preferred to avoid shift of S due to modest punch through in the device. The parameter extracted must make sense for the L_g of the device. DIBL is

extracted from the lateral shift of I_D (due to shift of V_t) as V_D is increased in the transfer curves in weak accumulation. DIBL is multiplied by intrinsic drain voltage (V_{Di}) in the expression for threshold voltage in the model. It can be extracted from the weak accumulation regime as shown.

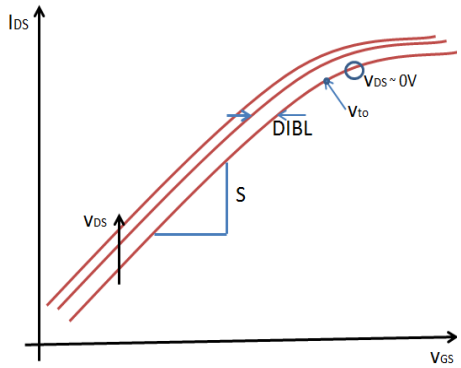


Fig. 11: Illustration of extraction of V_{to}, S and DIBL from transfer curves

Extraction of v_{sato}/v_{xo}, β (beta) and θ_v (vtheta), θ_μ (mtheta) and R_{th}

v_{sato}/v_{xo}, β and θ_v, θ_μ and R_{th} can be extracted from output characteristics. v_{sato}/v_{xo} can be fitted to get accurate match with saturation current level. v_{xo} extracted must lie between the bracket of peak electron velocity (2.5×10^7cm/s) and saturation velocity (1.3×10^7cm/s) depending on gate length. The transition from linear to saturation current in output characteristics is governed by F_{sat} which has a parameter β. β should ideally lie between 1.5-3 for these type of HEMTs depending on saturation.

η_v is thermal coefficient affecting velocity. They can be extracted from slope of output curves in saturation at large V_G where self-heating is dominant. η_v together with the thermal resistance (R_{th}) is directly responsible for the negative slope of the output curves and can be extracted from fitting. θ_v and θ_μ are also fitting parameters which affect V_{DSAT}. They can be extracted from V_{DSAT} at lower V_{GS} when self-heating has not yet kicked in. Thus by fitting to get correct linear-to-saturation transition voltages at larger V_{GS} we can get values of θ_v and θ_μ. R_{th} of the thermal network is also obtained in high bias-region where self-heating is predominant. Since R_{th} characterization through TCAD and evaluation of thermal coefficients through multi-temperature measurements has not been done yet, it has been reduced to a fitting parameter for now.

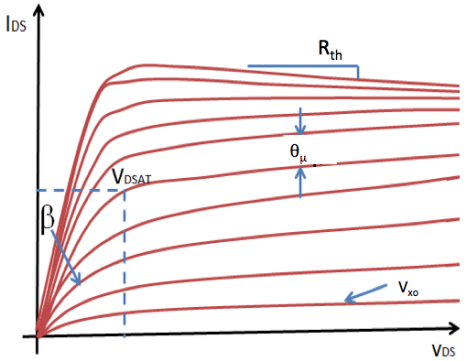


Fig. 12: Illustration of extraction v_{sato}/v_{inj}, β and θ_v, θ_μ, R_{th} and η_v from output curves

The implicit-gate transistors on the source and drain access regions should ideally have same transport parameters as that of other transistor regions. The short channel effect parameters and sub-threshold slopes of these regions are fitting parameters or can be extracted from TLM measurements. The key parameters for these transistor regions are the **cig** (implicit-gate capacitance) parameters, which affect the quasi-saturation behavior in high Vg regimes in the output characteristics.

Extraction of gate current parameters

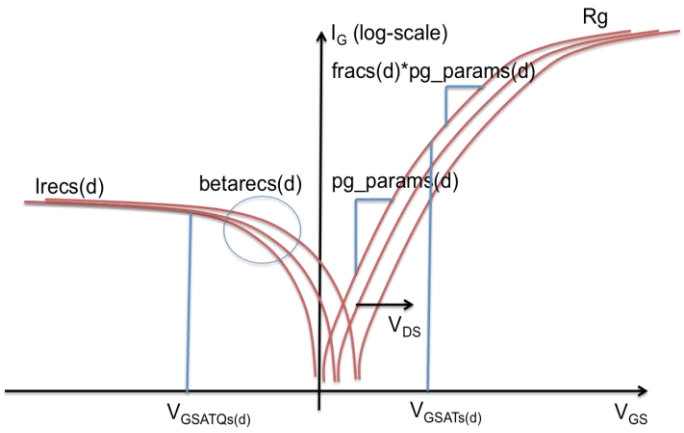


Fig. 12: Illustration of extraction gate current parameters from gate-current curves

The gate current parameters such as ideality factors (**pg_params(d), pg_param1**), reverse saturation currents **(irecs(d), ijg)**, along with reverse current parameters **(Vgsatqs(d), betarecs(d))** can be extracted from gate-current plots.

In addition to the parameters in the model, additional passives associated with the device such as terminal resistances, inductances and pad capacitances are critical to capture small and large signal device characteristics at RF frequencies. Since these device-level parasitics are layout and process dependent, it is not included as part of the model file. Instead they are to be added at the schematic level. While this is not necessary for power conversion applications and hence Toshiba HV-GaN HEMTs, it is critical for RF devices and for Qorvo device data for fitting S-parameter, power sweep, source and loadpull data. The schematic and values are in the ADS files are attached in the release. This section gives a rough idea of the model parameters of MVSG model and the regions of the terminal characteristics that are significantly impacted by these parameters for easy extraction.

MVSG_CMC – Phase IV model release files

CMC-phase4release-MVSG folder

This directory contains the **lib** folder and **model_qa** folder which contains the CMC test suites with DC, AC, noise tests. In addition it contains master Verilog-A files **mvsg_cmc.va** along with the extracted parameters as default parameters. The reference results are also placed for comparison.

lib folder

This directory contains the latest simulator files provided by CMC along with model-result comparison code and modelQA test routine.

Model_qa folder

This directory contains two sub-folders:

1. veriloga: This folder contains the Verilog-A model **mvsg_cmc.va** in the location:/veriloga/vacode/mvsg_cmc.va

2. mvsg_cmc: This has the sub-directories **mvsg1.0.0beta1/dmode/** that contain all the QA test suites along with the parameter set and reference results. The file structure is as follows:

i) parameters: dmodeParameters- This file contains the parameter model-card used for generating the test results.

ii) reference: This folder contains the standard test results that can be compared against other simulators. The reference results comprise of 14 DC simulations, 9 AC simulations, and 5 noise simulations. The DC tests are for nominal and different W/L combinations and include bias (V_D and V_G) sweeps and temperature sweeps. The tests turn different FPs on and off in order to test the various sub-circuit modules in the VA-code. The AC tests are primarily to test the CV characteristics of the model through V_G and V_D sweeps. The V_D sweep simulations turn different FPs on and off to test their contributions to the C_{iss}, C_{rss} and C_{oss} in off–state. The noise simulations are done at different bias and temperature dependencies.

iii) **Makefile:** This is the latest CMC provided makefile for running the QA tests.

iv) **qaSpec:** This is the release file that contains the various tests that can be run using the release package in different simulators to evaluate the model's performance in each simulator and compare the results with the standard results in the package.

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