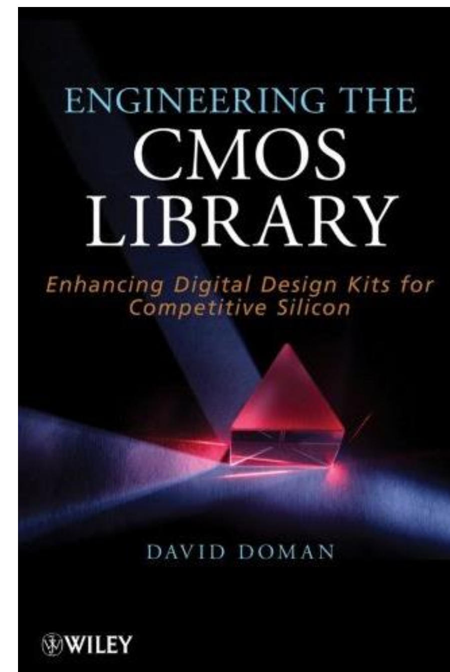
David Doman, GlobalFoundries

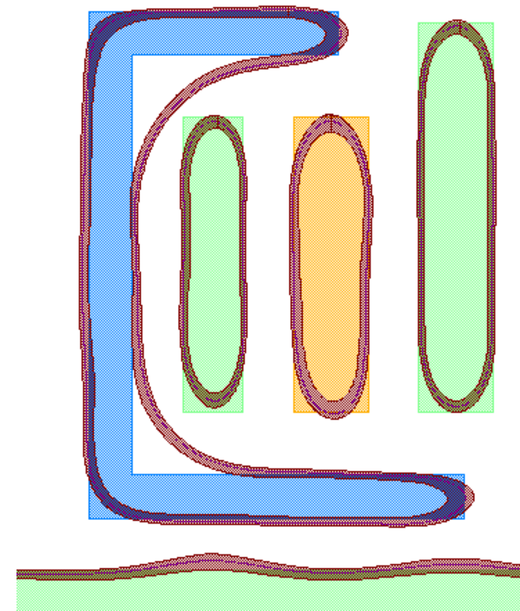
- 35+ years in industry (stdcell libs/DDKs & DRC/DFM)
  - 1.25micron down to below 10nm
  - Mainly digital, but dabbling in analog/mised signal, IO, memories
  - Author: Engineering the CMOS Library: Enhancing Digital Design Kits for Competitive Silicon (JWiley Press)
  - For standards committees, patents, publications: see my linkedin page



Scaling challenges for Interconnect Levels

- Multi-patterning needed to resolve feature sizes.
  - Triple or quad patterning needed.
  - No deterministic coloring solution exists for more than double patterned layouts.
  - Complex overlay and alignment strategy along with reduced overlay error margin, via-to-metal TDDB challenged.
  - Higher yield loss due to random defect density due to higher number of patterning steps.

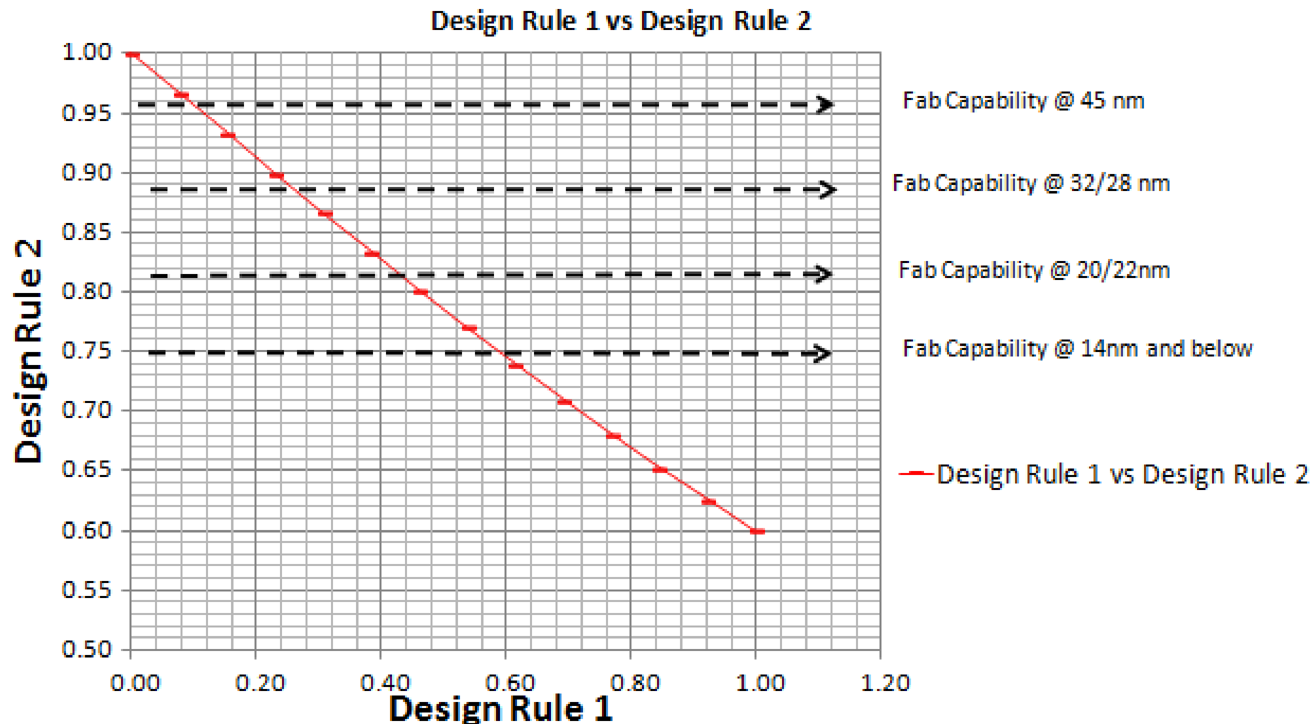
- Corner rounding & unidirectional SADP.
  - Optical corner rounding is not scaling.
  - Adopting unidirectional layouts causes simple wiring to use multiple levels (performance impact).
  - Fixed spacing (SADP) has performance impact due to parasitic capacitance.
  - Wider wires for power supply to high fan-out cells present forbidden pitch scenarios, litho printabilty issue.



Simulated litho contour show high corner rounding.

Scaling challenges for Contact levels

➢ Multiple contact shapes and local interconnect challenges.
- Increased interdependence between design rules.
- Need for more special contact shapes
- Meeting Process window is challenging
- Process Control also needs to improve with technology generation.
- Innovative process integration schemes and materials needed to meet the contact sizes for optimum scaling and performance benefits.
- Triple-patterning and quadruple patterning needs and its design challenges.



In General…

EDA vendors need to improve support:

- SADP, SAQP mandrel/spacer-- virtual design tools to assist in visualization of shapes and reduce design rule complexity

- 2-4 color advanced decomp that includes pattern matching, pitch/run length detection, smart coloring for balance and stitch placement.

- FDSOI design tools for back bias and antenna rule handling (source/drain antenna rules require routing tools to recognize these FD scenarios, not currently supported).

- Special construct handling-- improve DRC+ support (not preferred, designers still insist on hard DRC rules, this has introduced a significant complication in the design rules for special constructs which are predicted to go to other modules besides MOL).

- General improvement in supporting new design methodologies as we are very far away from the era of the shrink and advanced technologies are changing whole architectures and techniques that generally require a more flexible EDA vendor to support designers and improve PDK quality.