



GaN HEMT SPICE Model Standard for Power & RF

Samuel Mertens
Si2Con
San Jose, CA
October 6, 2015

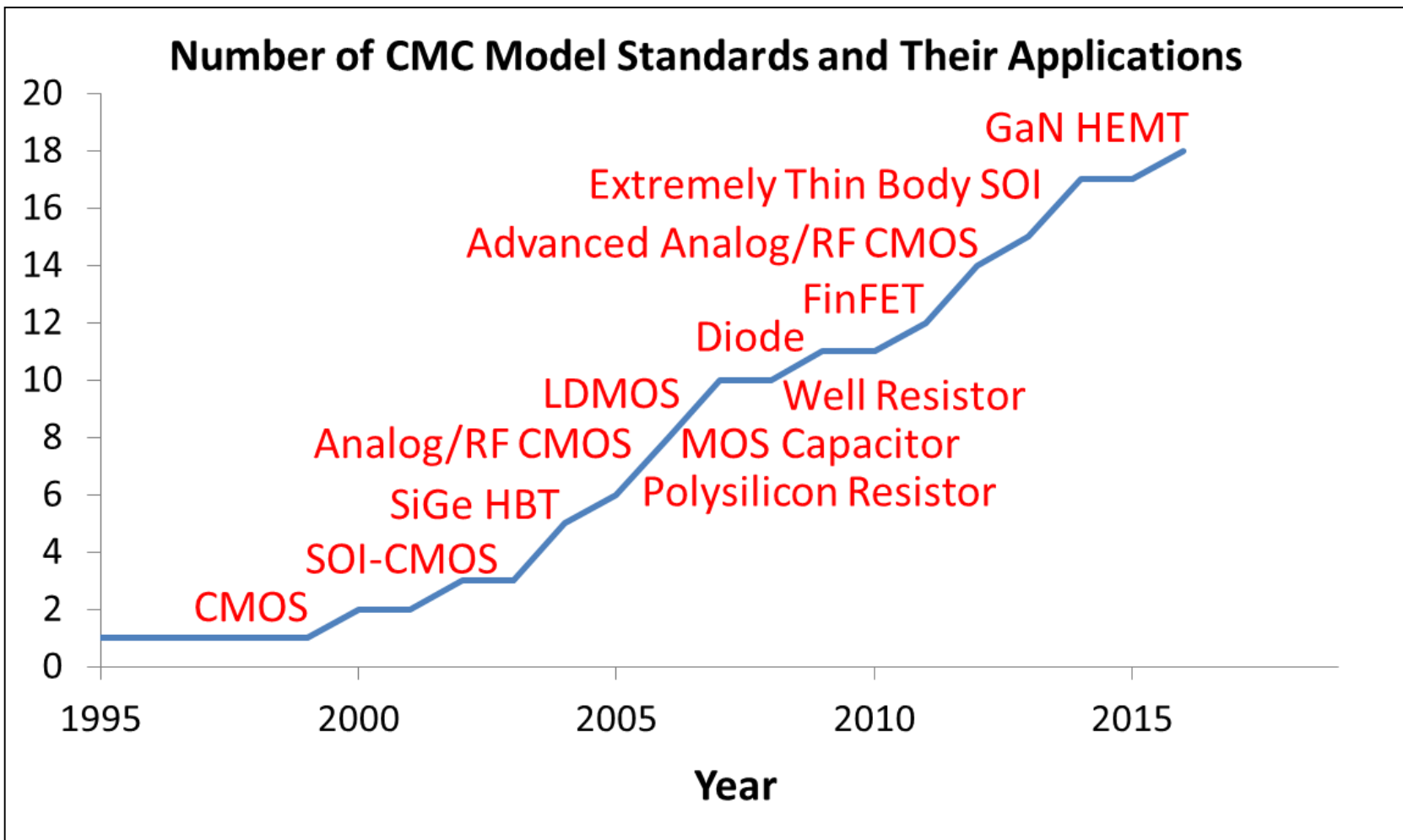
cādence[®]

Compact Model Coalition @SI2

- Standardizing Compact Models
 - Since 1996
 - Started with BSIM3
- Support standardization and making the model usable by industry
- GaN HEMT first foray into III-V semiconductors



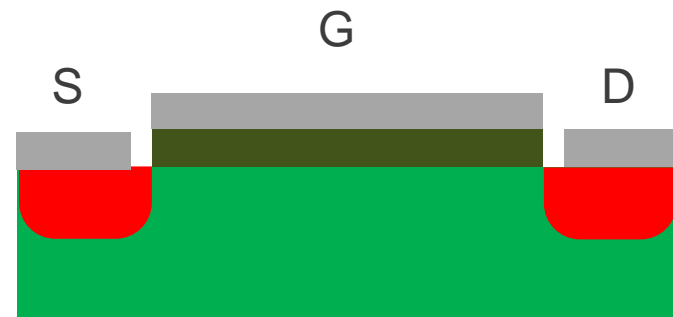
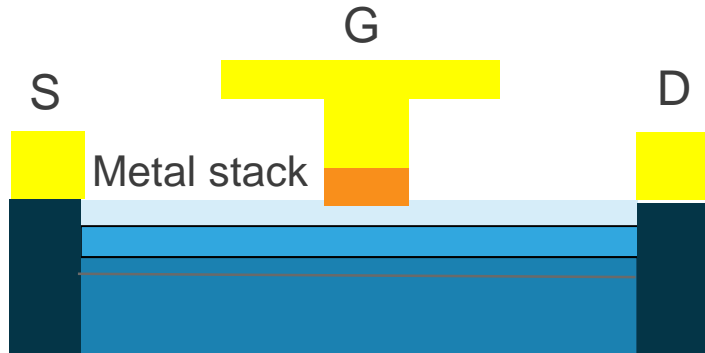
CMC Progress Chart



Plot courtesy of Green

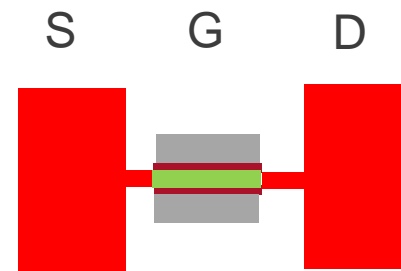
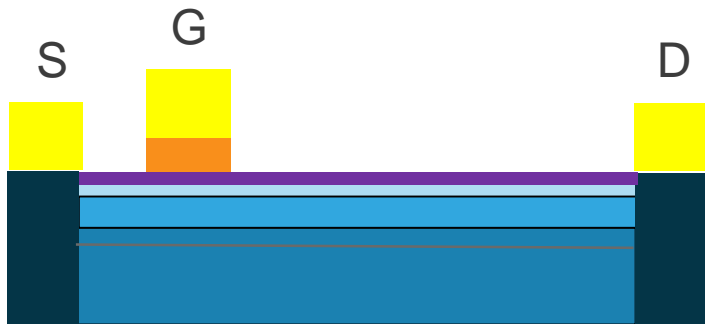
HEMT vs MOSFET (really old) view

HEMT	MOSFET
Schottky gate M-S	MOS-gate Si/SiO ₂
2DEG	Inversion layer
III-V or II-VI	Si
Always on (gate turns device off)	Easy control of V _{th}
Only n-channel	N- and p-channel (CMOS)
Expensive	Inexpensive
Reliability issues	Reliable
Trapping important	No issues with traps



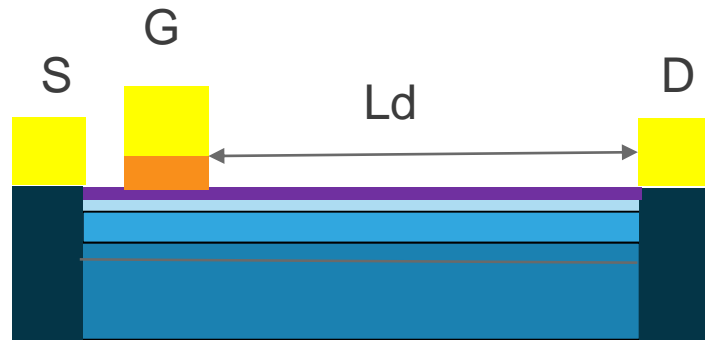
HEMT vs MOSFET – how it is now

HEMT	MOSFET
Schottky gate M-S or M-I-S (using deposition)	High K-dielectric gate (not SiO ₂) using deposition
2DEG	Inversion layer
III-V or II-VI	Si or combination with (Ge or C)
Depletion mode and Enhancement mode possible	Easy control of V _{th}
N-channel, no good p-channel	N- and p-channel (CMOS)
Expensive, but cost is improving	Inexpensive (but not for small volume)
Reliability concerns but improving	Reliable, but is more of a concern
Traps still an issue	No issues with trapping (except for LDMOS aging)



GaN vs Si

- GaN higher bandgap (3.4 eV) than Si
 - Very high critical field which enables a much smaller on-resistance (shorter drift region)



GaN vs Si

- 2DEG HEMT structure and GaN material properties allow for high electron mobility and current in GaN HEMTs
- Thermal conductivity similar to Si
 - GaN can operate at higher temperatures

Historically, III-V semiconductors used to live only live in RF

- Higher Electron-mobility at high electron density of III-V (including GaN) leads to higher operational frequencies and lower losses
- Not negligible market-wise
 - GaAs PA are part of most cell phones
- The complexity of the chips are smaller
- Main simulation focus is in frequency domain

III-V industry has been relatively free of standard models

- **Historic reasons**
 - In-house fabrication
 - Small # of transistors
 - Frequency domain
- **Proprietary models**
 - Based on public model, but with improvements
 - Considered a competitive edge
- **Limited tools needed**

GaN in Power Electronics – since 2009

- Reduced power losses for switching applications
- Low gate charge, and low on-resistance lead to many commercial application for power conversion (and no QRR)
- These companies are used to Si integration and Si flow
 - Standard models are part of that flow
 - Time domain is important
- No body – no inversion, no accumulation can't use Si model

Compact Model primer

- **Types of models considered**

1. Empirical

- Mathematical functions are fit to the I-V and Q (or C)-V measurements

2. Threshold Voltage based

- Physical behavior of I-V and Q-V are fit to functions, derived from approximate solution of the underlying physics, using the threshold voltage as a fitting parameter

3. Surface-Potential (or charge-based current) based

- Surface-Potential (or charge) is calculated out of which currents and charges are derived

CMC standardization procedure

- **Four phases**
 1. Call for models
 2. Self-Evaluation
 3. **Evaluation by CMC members**
 4. Prepare Standard

Phase 1 details

- CMC compiled a list of requirements
 - Technical requirements
 - Support requirements
- We received 9 applications who returned a checklist and a list of references
- Committee reviewed the applicants

Phase 1 requirements - highlights

- Technical requirements
 - Physical
 - Surface-Potential based (preferred)
 - Gummel-symmetry
- Support requirements
 - Documentation
 - Support
 - Maintenance

Phase 1 progress

- 8 were invited to present at the Q4'13 CMC meeting
- Anwar (Uconn), Angelov (Chalmers), Antoniadis (MIT), Chan(UST), Khandelwal (UNIK), Martin (LETI), Shur (RPI), Trew (NCSU)
- 4 candidates found a sponsor to move to next phase

Phase 2 candidates

- Angelov (Chalmers)
 - Semi-empirical, semi-threshold voltage based
 - Current “standard” in RF
- Antoniadis/Radhakrishna - MVSG (MIT)
 - Charge-based current calculation
- Khandelwal – ASM-HEMT (UNIK)
 - Surface Potential based
- Martin – HSP (LETI)
 - Surface Potential based

Phase 2 details

- Two sets of measurement data were supplied
 - Qorvo (RF)
 - Toshiba (Power switching)
- The 4 candidates were asked to fit this data to their model and then show overlays for a list of plots

Phase 2 ballot results

After ballot 2 candidates are being reviewed by CMC membership in phase 3

- Antoniadis/Radhakrishna – MVSG (MIT)
- Khandelwal – ASM-HEMT (UNIK)

Really strong candidates for both RF and power switching applications

Phase 2 data

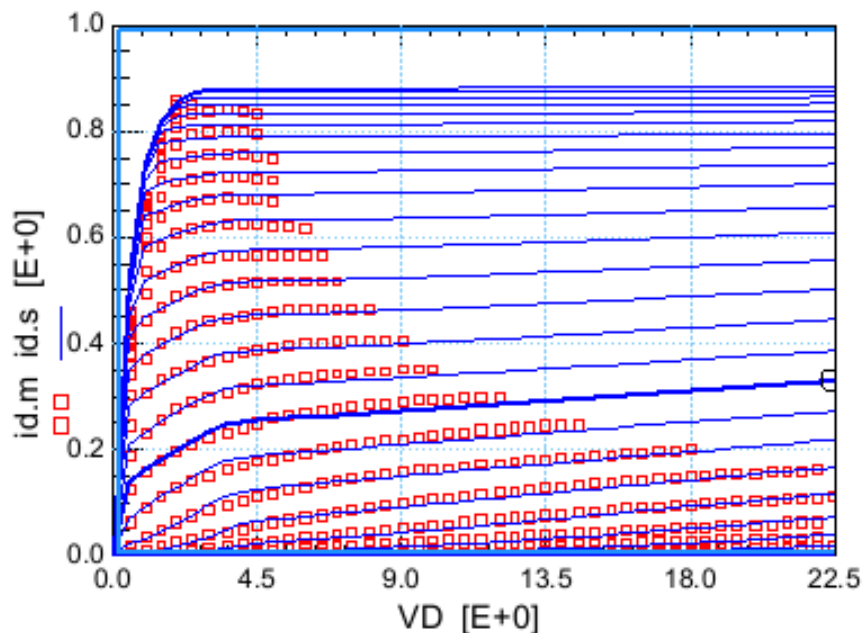
- RF (Qorvo)
 - DC I/V
 - Pulsed I/V
 - S-parameters
 - Power Sweep
 - Load Pull/Source Pull

Pulsed I-V

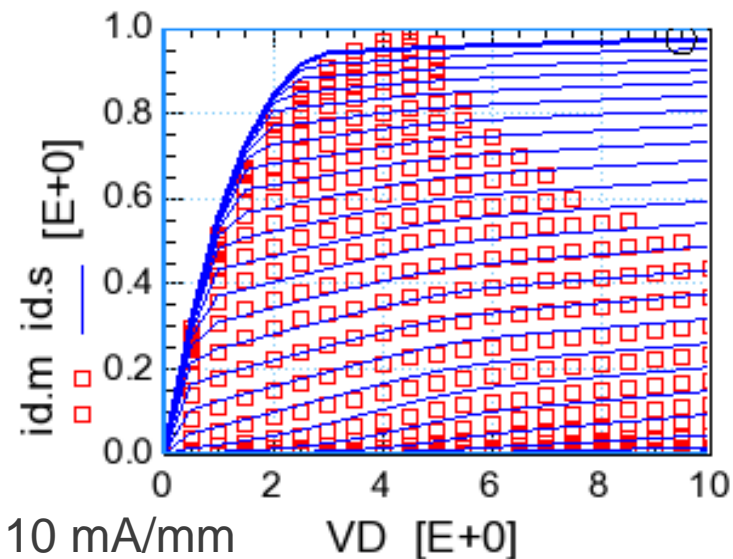
- Pulsed I-V measures I-V using short pulses starting from a quiescent operating point
- Allows one to measure effect of selfheating and trap states
- Self-heating is important at high drain voltage/current
- Traps (depend on the bias condition) affect the output characteristics and cause the knee walk-out

Knee walk-out

- RF device DC I-V and pulsed

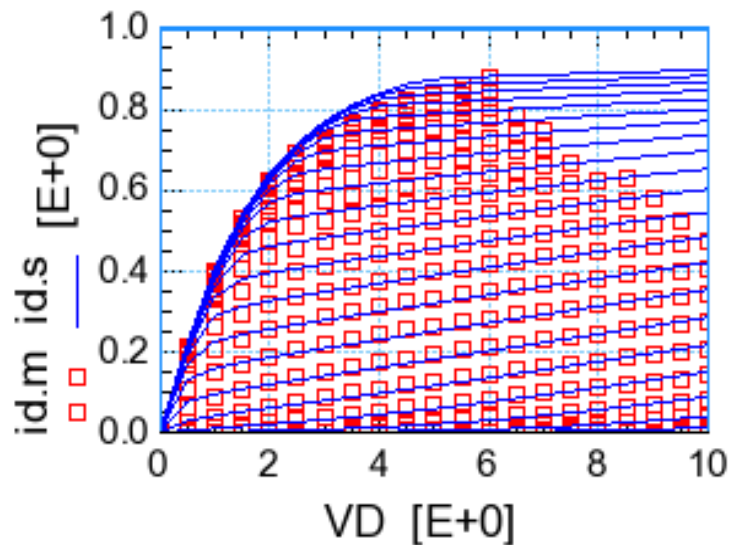


Plots courtesy of Radhakrishna



5 V and 10 mA/mm

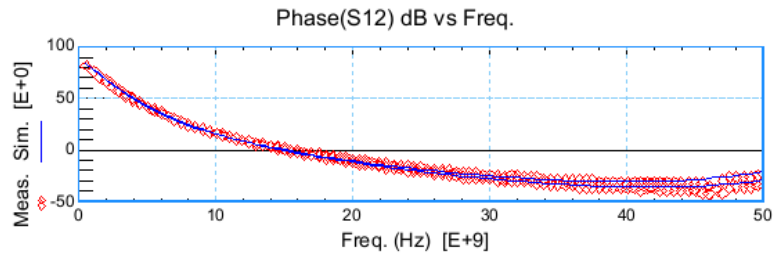
VD [$E+0$]



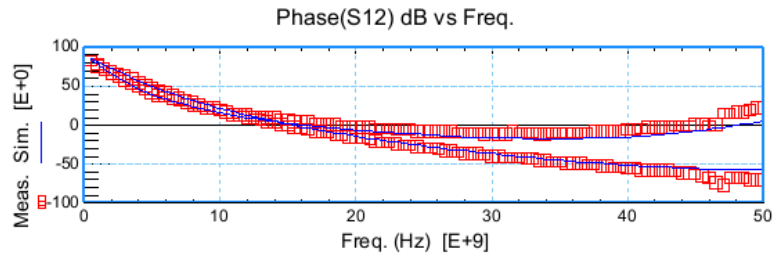
20 V and 100 mA/mm

VD [$E+0$]

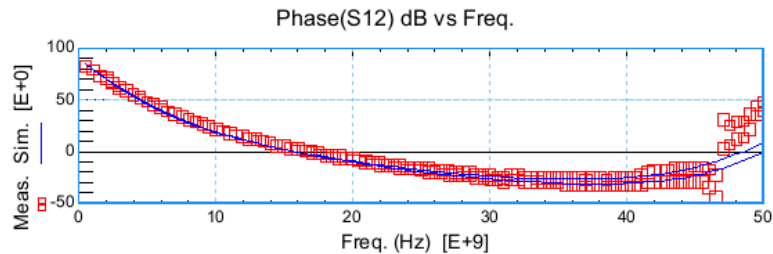
S-parameters



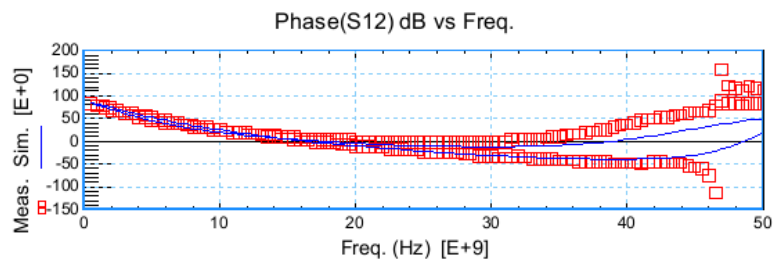
Plot EG0490_8x40_W3_1514_dc_Sparms/AC_at_All_Vds_Vgs/Sparms_VD5_10_100mA/Phase_S12



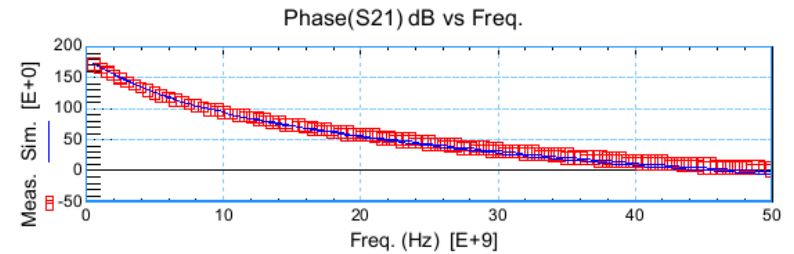
Plot EG0490_8x40_W3_1514_dc_Sparms/AC_at_All_Vds_Vgs/Sparms_VD10_10_100mA/Phase_S12



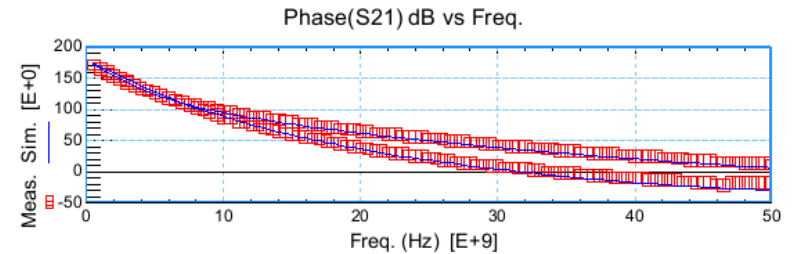
Plot EG0490_8x40_W3_1514_dc_Sparms/AC_at_All_Vds_Vgs/Sparms_VD15_10_100mA/Phase_S12



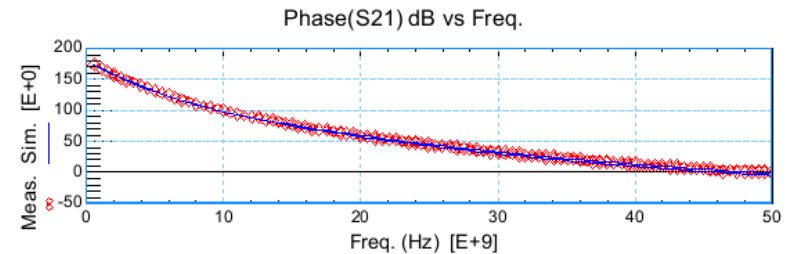
Plots courtesy of Khandelwal



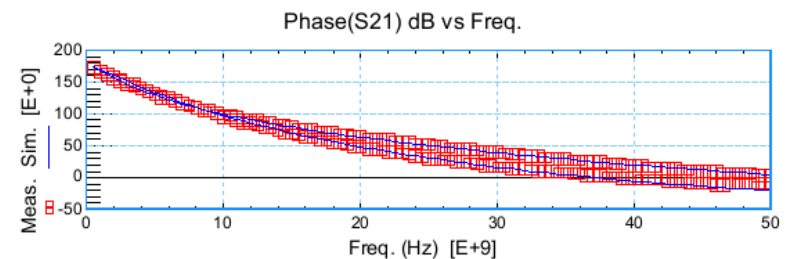
Plot EG0490_8x40_W3_1514_dc_Sparms/AC_at_All_Vds_Vgs/Sparms_VD5_10_100mA/Phase_S21



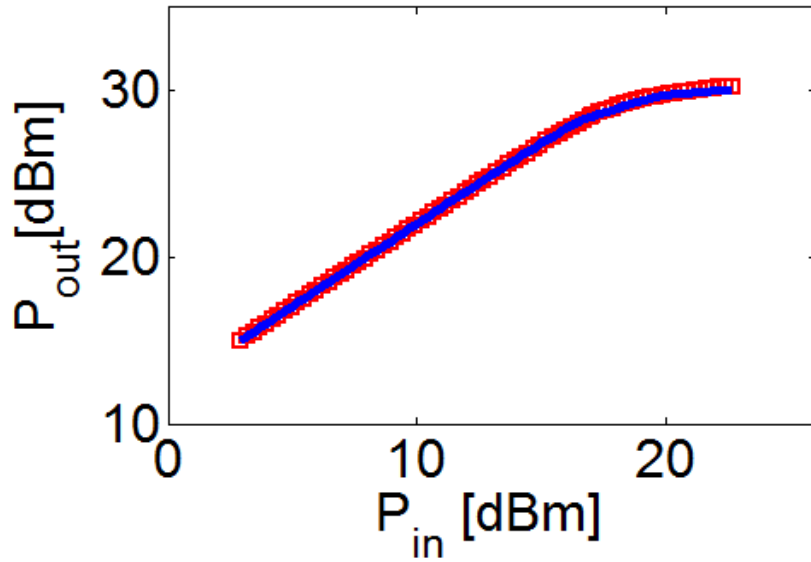
Plot EG0490_8x40_W3_1514_dc_Sparms/AC_at_All_Vds_Vgs/Sparms_VD10_10_100mA/Phase_S21



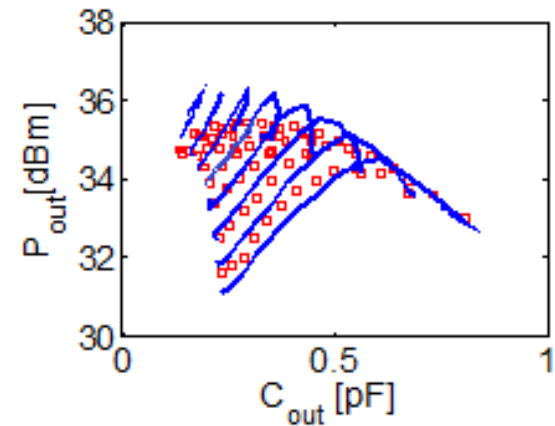
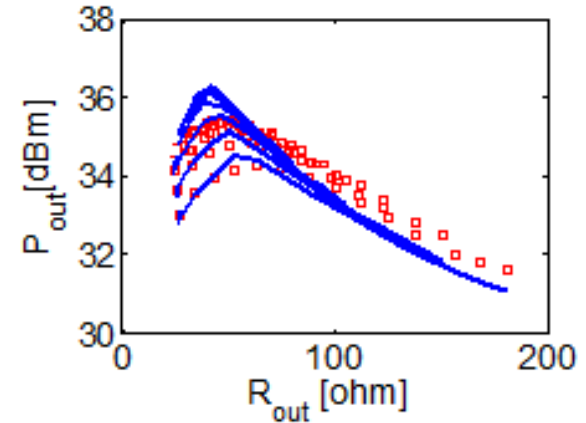
Plot EG0490_8x40_W3_1514_dc_Sparms/AC_at_All_Vds_Vgs/Sparms_VD15_10_100mA/Phase_S21



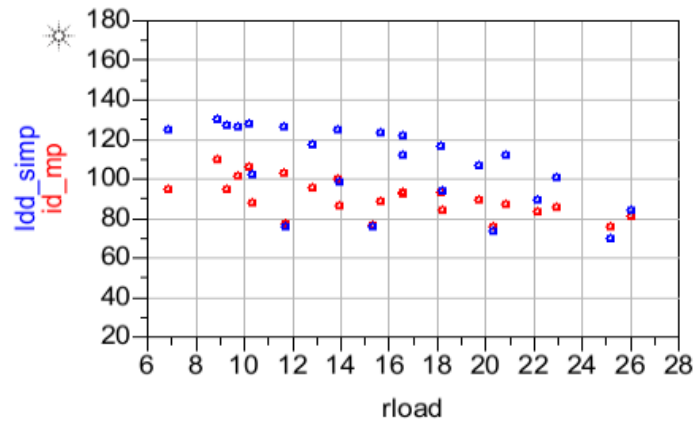
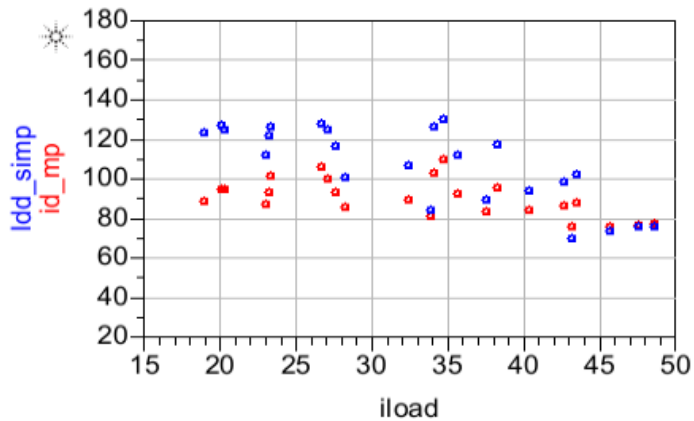
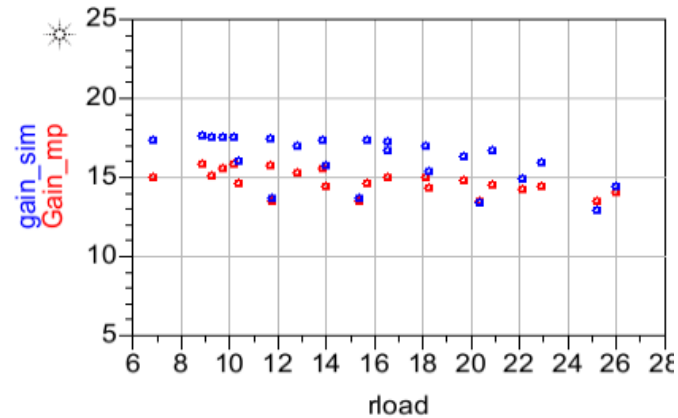
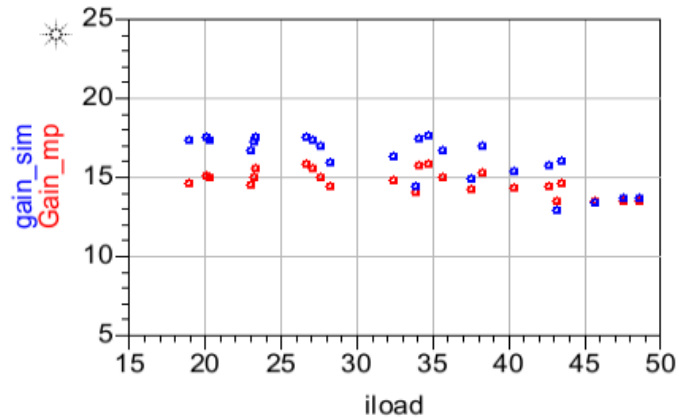
RF measurements – power sweeps



Plots courtesy of Radhakrishna



Source sweep

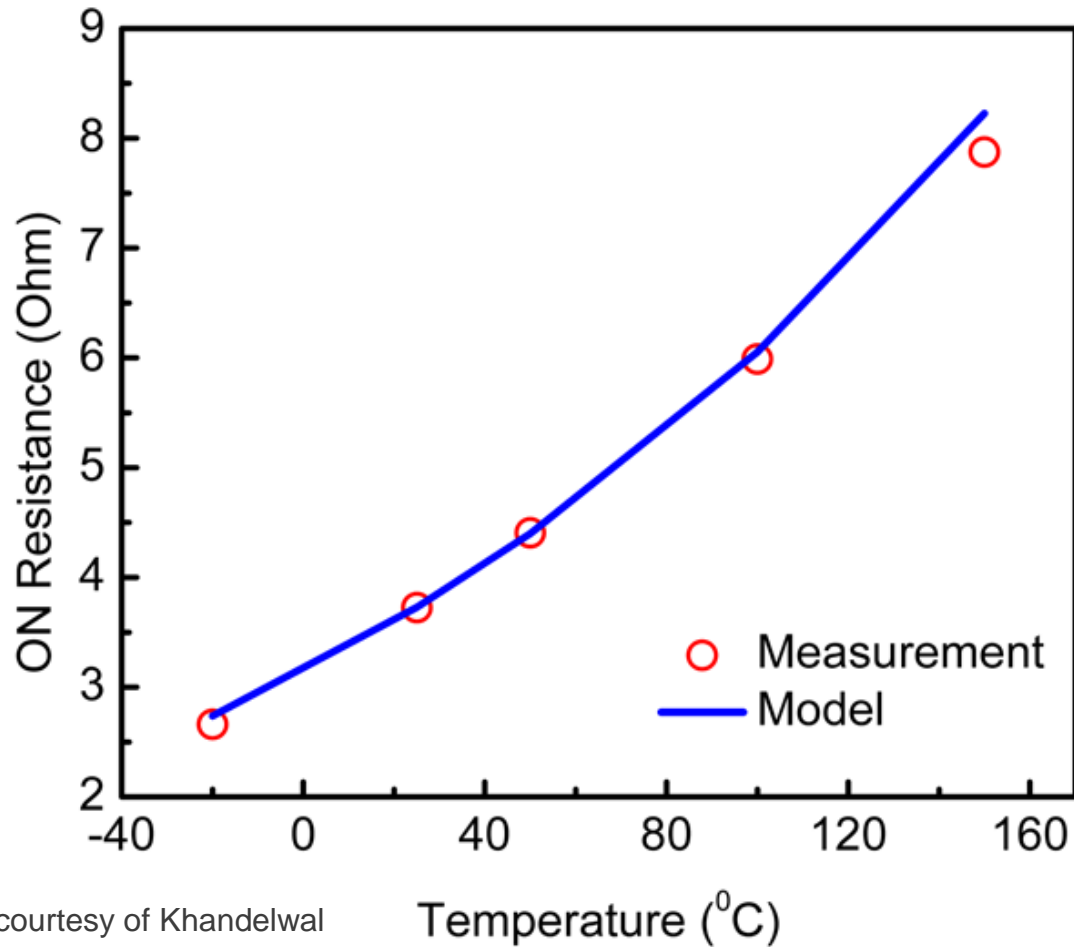


Plots courtesy of Khandelwal

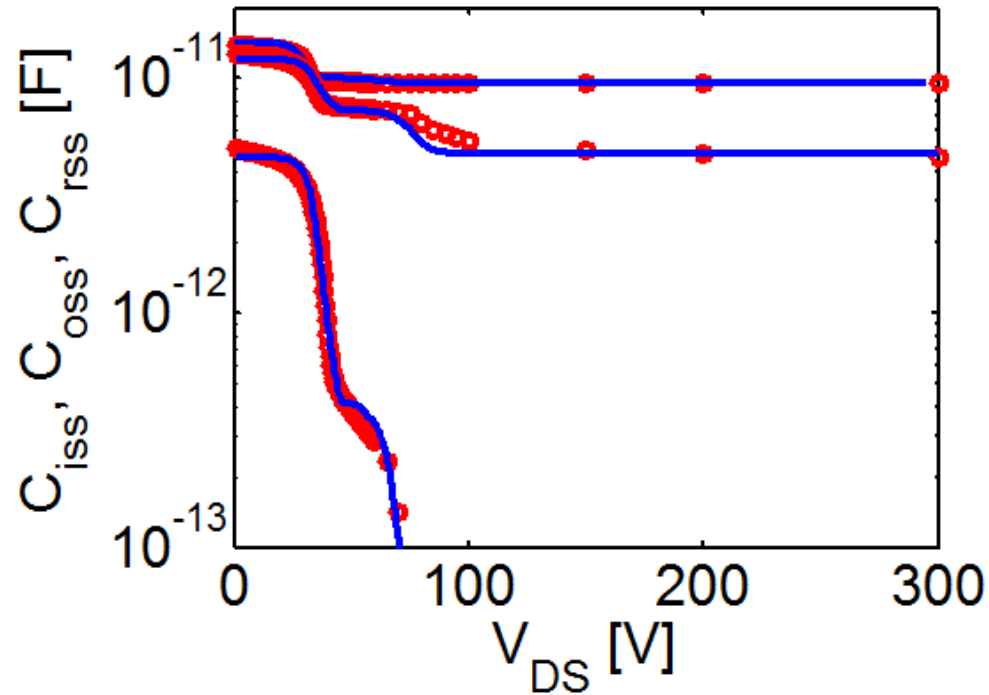
Phase 2 data

- Power switching (Toshiba)
 - DC I/V vs. Temperature
 - C/V
 - Switching Collapse
 - Gummel symmetry/McAndrews Symmetry test

On-resistance vs. Temperature

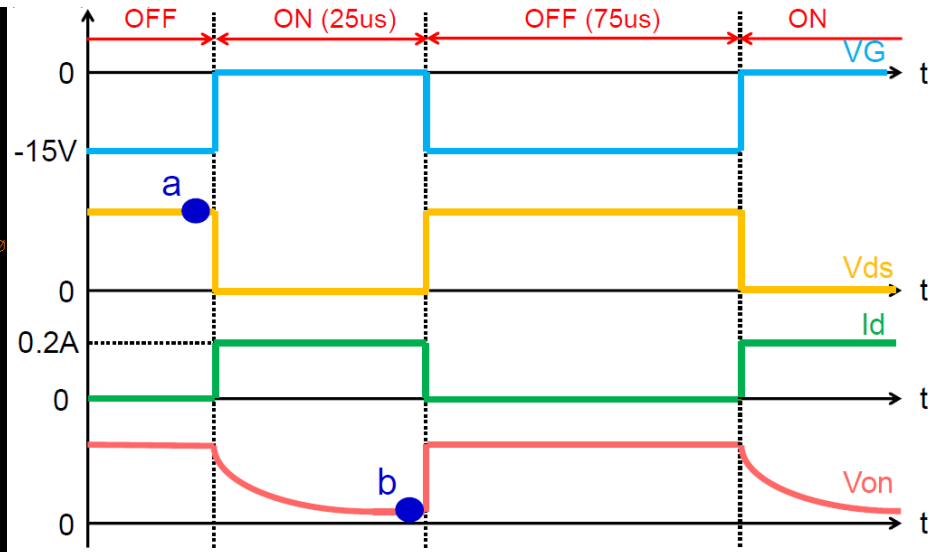
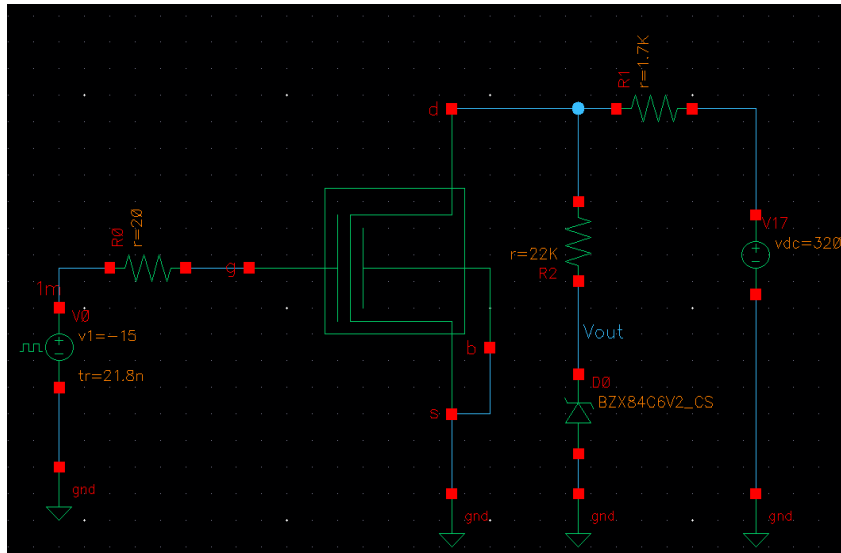


Capacitances vs. Voltage



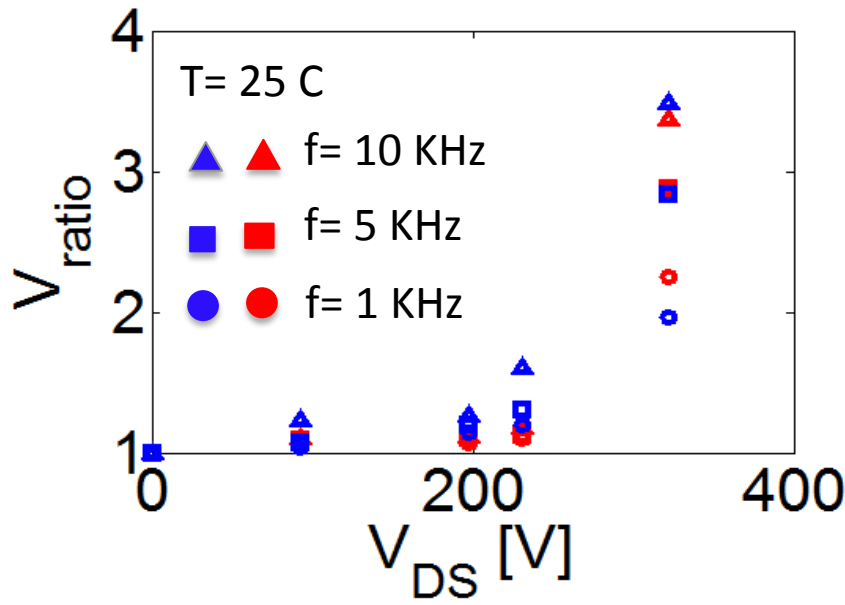
Plot courtesy of Radhakrishna

Switching collapse characteristics definitions

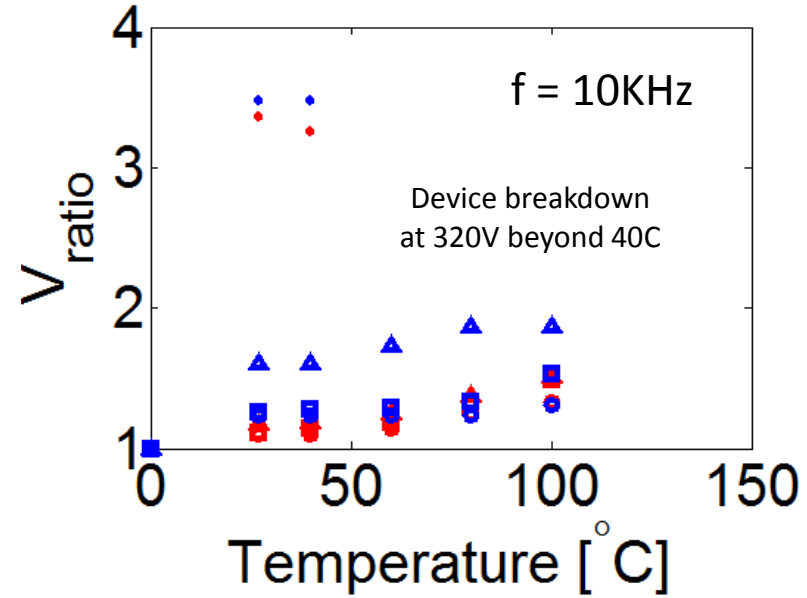


Plots courtesy of Radhakrishna

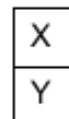
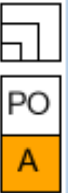
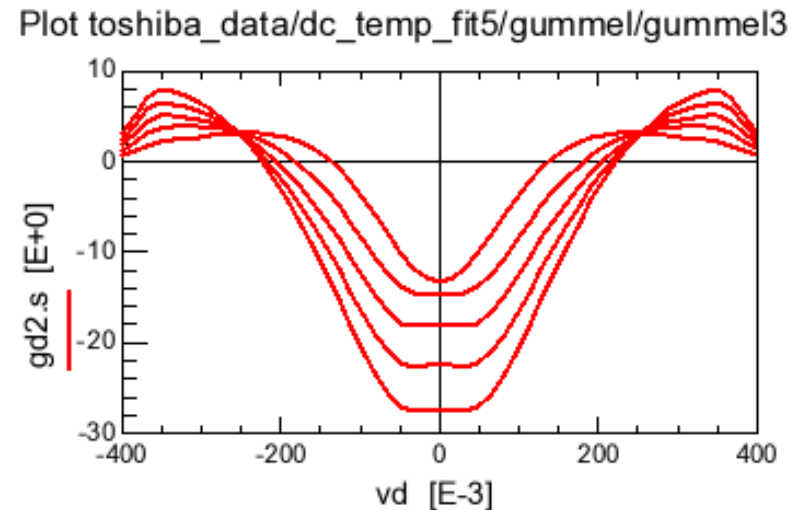
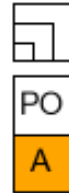
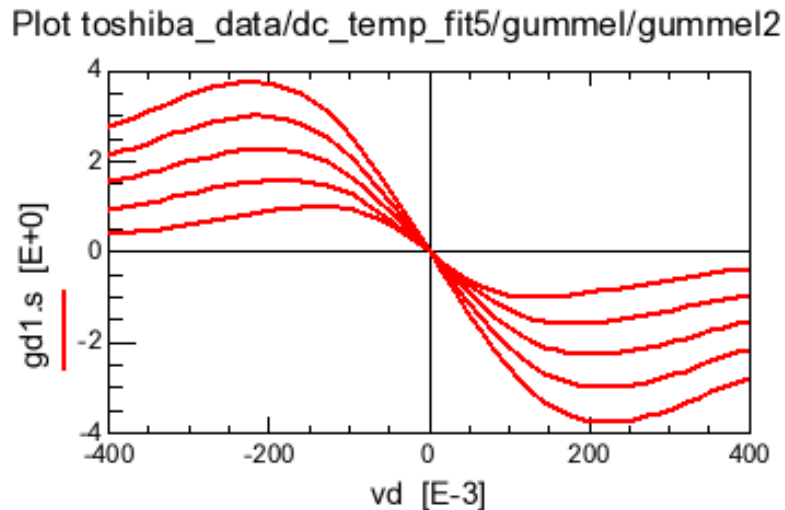
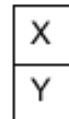
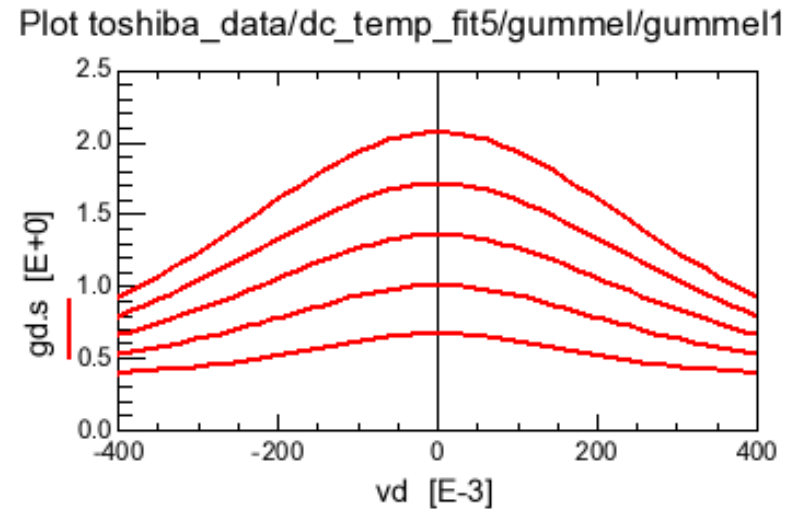
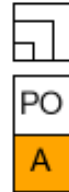
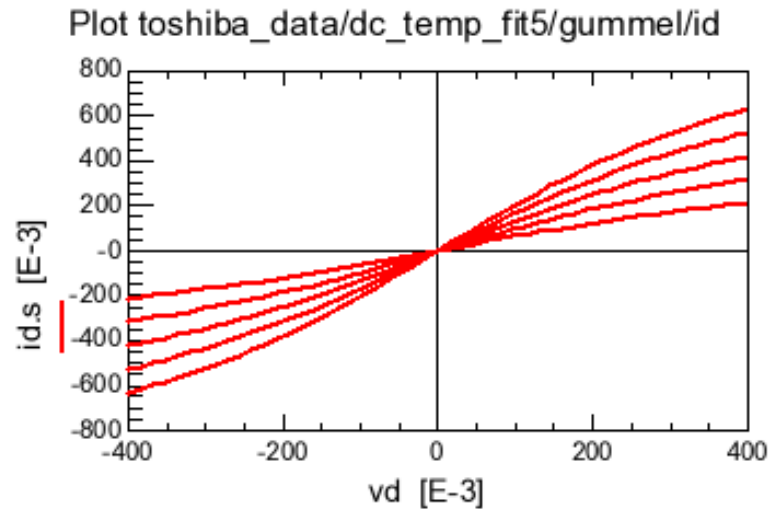
Switching characteristics



Plots courtesy of Radhakrishna



Gummel Symmetry - Toshiba



Plots courtesy of Khandelwal

Phase 3

- **CMC members received**
 - Model code (Verilog A)
 - Documentation
 - Extraction procedure
 - Parameters sets
- **Testing model**
- **Ballot (Q2 '16)**

Phase 3 testing

- Extraction on their own devices
- Circuit simulation
 - Larger circuits
 - Convergence
 - Performance
 - Time and Frequency domain
- Noise testing
- Usability

Phase 4

- Model is made ready for standardization
 - QA suite
 - OP parameters
 - Clean up
 - Clear final code
- Could take 1-2 quarters
- Standard model at end of 2016

CMC

- Join CMC to help us define this standard

Acknowledgements

- All model candidates for their hard work
- Ujwal Radhakrishna (MIT) and Sourabh Khandelwal (UCB) for letting me share their plots
- CMC members
- Qorvo and Toshiba for the HW data
- James Fiorenza (ADI), Vijay Krishnamurthy (TI) and Rob Jones (Raytheon), Keith Green (TI)

cā dence[®]