Si2 Newsletter

OpenPDK Architecture

- Foundry
- Design Parameter Database (Open Format Based)
- User
- Format Generators
- Existing Input Data Formats
- Callback Parameter Types (Not actual values)
- PDK Dev. Flow₁
- PDK Dev. Flow₂
- PDK Dev. Flow₃
- PDK Dev. Flowₙ
- OA Symbols Enh.
- OA Tech File Enh.
- OA API
- OA DB
- New standardization work
- DRC/LVS Engine
- OpenDFM w/ Targeting
- SPICE Socket
- SPICE Engine
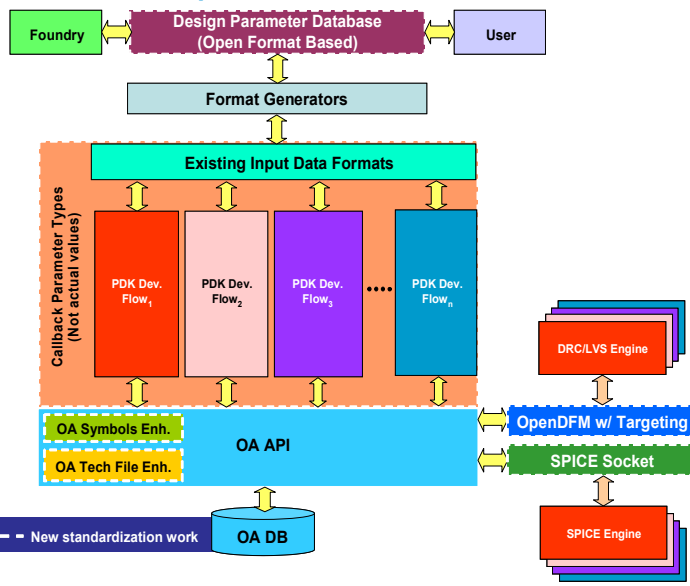
OpenPDK Groups Get to Work

Officers Elected - Working Groups Formed

The OpenPDK Coalition was formed to satisfy a critical need for open standards representing the different components and parameters that are needed in generating PDK's. Si2 has been tracking this part of the semiconductor ecosystem for several years and has maintained an ongoing dialog with Si2 members and domain experts to determine the right moment to begin a project such as this. Based on all the feedback received, that moment has arrived.

The overarching goal of the OpenPDK Coalition is defining a set of open standards to allow a PDK to be as portable across foundries and as agnostic to EDA tools as possible. The Si2 OpenPDK will enable greater efficiency in PDK development, verification and delivery and will provide equivalent support to foundries, EDA tool vendors, IP providers, and end users.

The Coalition will define new standard specifications at the PDK development environment level, as well as standards for delivery of a populated PDK file set. These will include: standardized format/database for foundry-provided process rules/information, standard API/format to capture the types, syntax and semantics of parameters that drive PDK generation/re-generation, standardized API to interface with engines for DRC/LVS/ etc with targeting enhancement, and standardized socket to access SPICE engines.

Phase 1: Addressing Immediate Stake Holder Interests

o Symbols, Callbacks & CDF Specs Standard
o eDRM Standard
o OpenDFM with Targeting for pre-OPC polishing
    OpenDFM defined operations and multi-vendor parser support.
    Open PDK can now determine how best to apply these ops. (LVS & PEX)
o SPICE Socket Standard
o Data base symbol standards - Expansion of the current standardized set.

Coalition Officers Elected

The OPDK Coalition members have also elected officers to guide the technical progress of the group. They are:

Coalition Chair: Matt Graf - IBM
Coalition Vice-Chair: Linda Fosler, Mentor Graphics
Technical Steering Group (TSG) Chair : Ravi Rao, Synopsys
TSG Vice-Chair: Gilles Namur, STMicroelectronics

15th Si2/OpenAccess+ Conference

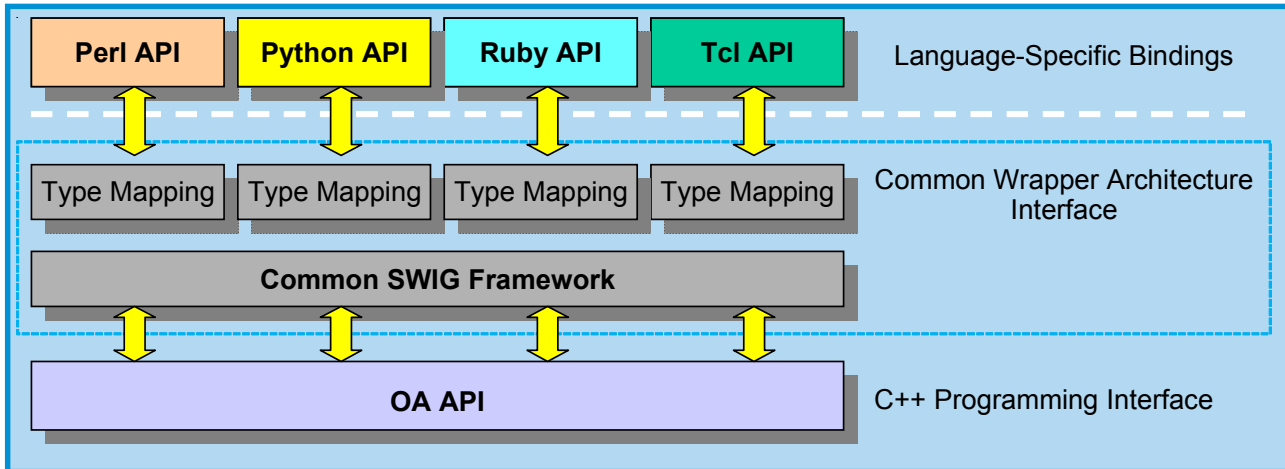### *Wednesday,October 20 at TechMart -Network Meeting Center, Santa Clara, CA.*

This conference will cover the increasingly inter-related areas of OpenAccess, Design for Manufacturability (DFM), Low Power design and the newest Coalition for Open PDKs. Updates on the industry adoption of OpenAccess will be presented along with status and plans for the future for all coalitions. Semiconductor companies and EDA vendors who have adopted Si2 standards will discuss their advanced capabilities and their experience. John Bruggeman, Senior Vice President and Chief Marketing Officer of Cadence Design Systems will provide the keynote address. The detailed agenda and registration informationis located at this link: http://www.si2.org/?page=1262

There will be a DFM session which will cover the first-ever meta language standard, OpenDFM, which describes DRC and DFM checks in a tool-agnostic fashion. The session will also include a presentation on the concepts driving process targeting which is becoming a key enabler for technology nodes at 32nm and below. Another session will cover the exciting new activity in the industry on truly open Process Design Kits. This Coalition has taken off very rapidly due to the pent up demand in the industry for standards at this fundamental level of design. In addition, OpenAccess is growing dramatically and is now a "must have" for all industry players and the talks in this session will highlight relevant experiences. A session on low-power design will discuss recent Low Power Coalition work in power modeling standards, and user presentations on lower design efforts at ARM and Renesas Electronics Corp.

As in prior conferences, there will be an evening session that will showcase demos of advances based on the technologies offered by Si2. This session will also serve as a valuable opportunity for networking. Refreshments will be served.

OpenAccess Coalition

Scripting Languages Working Group

Perl API | Python API | Ruby API | Tcl API | Language-Specific Bindings

Type Mapping | Type Mapping | Type Mapping | Type Mapping | Common Wrapper Architecture Interface

Common SWIG Framework

OA API | C++ Programming Interface

The OpenAccess Coalition Scripting Languages Working Group (WG) has created interfaces between the OpenAccess C++ API and the 4 most popular open scripting languages - Perl, Python, Ruby and Tcl. This WG has defined a common architecture for the different language translators, and has simplified and standardized the building and maintenance of scripting language interfaces as much as possible. Most OpenAccess API methods should now be supported without hand coding through templates, code generators, etc.

The group has also provided suggestions to the OpenAccess ChangeTeam about API changes that would make the different scripting language interfaces easier. Guidelines for each language will include means by which it may be true to the OA interface (docs for OA C++ interface should match each language API closely) and being true to the native language look-and-feel (iterators, exceptions, etc. done in a native way). The working group is still recruiting interested companies and individuals. If you have an interest, please contact nenglish@si2.org for more information.

The Architecture and implementation under development & review
• Alpha release (ChangeTeam members only):   Target: 08/31/2010 (Completed)
• Beta release (OpenAccess Coalition only):   Target: 10/31/2010
• OpenAccess labs being ported from C++ to support all 4 scripting languages
• Download licensing: OpenAccess v4 for scripting language wrappers & bindings

Multithreading in OpenAccess

The availability of workstations and servers powered by multi-core processors provides an excellent opportunity for solving many of the hard-core chip design and analysis problems at the newest technology nodes. These problems require significantly greater capacity and speed, i.e., what is needed are multi-threaded applications that are implemented on an infrastructure that supports multi-threading (MT).

MT is fraught with problems and pitfalls. Thus, support for MT in OpenAccess requires careful analysis of the different use cases to determine a series of deliberate steps forward so that in the process of moving forward, we do not create a version that corrupts the data in one scenario due to the effects from another. So, the plan is to support a general interface that would support various types of MT, but within this framework support first some specific, well-understood use cases for now. As more experience is gained with the first implementation and more use-cases are defined, MT support will be expanded to provide greater and greater capability.

MT requires a locking mechanism, particularly in "multiple-read/write" mode, to ensure data integrity and to prevent multiple applications from changing the same data at the same time. So. the first release will not only include a native locking mechanism but also a special OpenAccess plug-in interface to allow any user of OpenAccess to plug in his/her own data locking mechanism as a replacement for the native version.
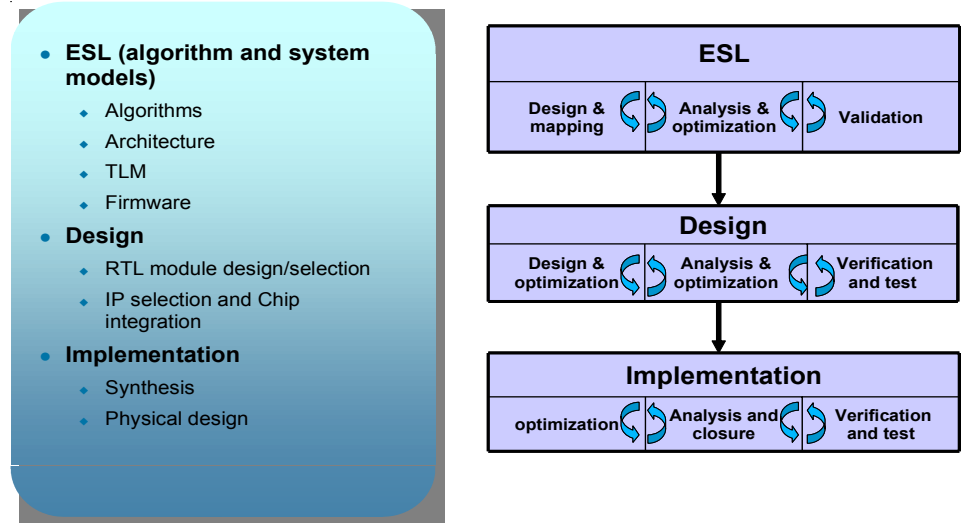
Power Modeling Standards

The Si2 Low Power Coalition has promoted and deployed a comprehensive Low Power Design Flow recommendation encompassing System-Level Design all the way through Implementation and tape-out. However, this flow requires the availability of suitable power models for each of the design phases. In particular, the models must enable power tradeoffs during system level design and simulation as well as support RTL design and implementation tasks such as RTL and gate level power analysis and optimization. Simply put, the need is for a single model that can be used at any and all levels. Or, as close as we can get to that ideal.

While power modeling capabilities exist today and are reasonably sufficient for modeling low level standard cell complexity, those capabilities are insufficient for modeling more complex objects. In particular, it is generally difficult to impossible to create accurate and complete power models for any IP block exhibiting more than simple power behavior using existing modeling capabilities; and, some new modeling structures are needed to model big blocks. Aside from accuracy and completeness, for any high level model to be effective it must be transportable between applications (such as pre-design estimation, TLM simulation, RTL simulation, etc.). Finally, the modeling techniques should be usable across different types of IP and not require different modeling technologies for different IP types.

Three Phases of the Power Aware Flow

These issues, among others, have motivated the Si2 Power Modeling Working group to identify new capabilities necessary for modeling IP blocks with a sufficient level of accuracy and flexibility so as to be useful in a comprehensive power aware design flow. For instance: The existing power state modeling capability in Liberty requires that all power states be mutually exclusive. The ability to represent either mutually exclusive or non-mutually exclusive states is necessary to efficiently model complex IP blocks because:

- Large IP blocks have many internal states.
- Large IP blocks are often composed of subcomponents, each with their own power states.
- For blocks with a substantial number of power states, requiring that the states be modeled in a mutually exclusive manner can cause state explosion.

- **ESL (algorithm and system models)**
  - Algorithms
  - Architecture
  - TLM
  - Firmware
- **Design**
  - RTL module design/selection
  - IP selection and Chip integration
- **Implementation**
  - Synthesis
  - Physical design

The Si2 Low Power Modeling Group is in the process of making recommendations to improve the power modeling capabilities of existing standards such as Liberty. The version 1.0 High Level Power Modeling Requirements addressing mutually exclusive and non-mutually exclusive power states has been published and is available at https://www.si2.org/openeda.si2.org/project/showfiles.php?group_id=76#p115. Version 1.1, that will be published in November, 2010, will address additional power modeling requirements. This is a significant addition to the state of the art in power modeling and even more powerful capabilities in power variability modeling are being considered. Please contact Nick English, nenglish@si2.org for more information.

New Tools from OCP-IP

The OCP-IP, a "sister" standards body to Si2, has recently released the following:

Virtual Platform Demo: Created utilizing OCP-IP's advanced Modeling Kit. This example platform acts as a guide to OCP-IP members enabling them to quick-start their ESL activities using the OCP-IP TLM Modeling Kit; which is fully compatible with OSCI's TLM 2.0.1. Both the kit and Virtual Platform examples are free to both OCP-IP members and non-members:: http://www.ocpip.org/vp_package.php

Transaction Generator: A transaction level (TL) SystemC simulator for benchmarking network-on-chips (NoCs) used in multiprocessor system-on-chip applications. Utilizing this tool makes simulation of larger systems substantially faster and the results obtained at this higher level can be accurately used as an initial estimate in selecting and fine-tuning NoCs: http://www.ocpip.org/tg_package.php

Standards Viewpoint

Who Should be Involved in Developing Standards?

Successful standards are a reflection of changing business trends. For example, the success of OpenAccess was mainly due to growth in custom semiconductor design and data complexities when building flows to support custom design. As power, thermal, and battery life issues became the bottleneck in many consumer-era IC designs, the LPC and CPF/UPF standards emerged. The industry's latest renewed focus on analog design automation in the inter-dependent fabless-foundry model drove the OpenPDK Coalition. Of course, I could also cite dozens of other examples all across the design flow – from Verilog to UVM – all reflecting needs and priorities of the times.

It's not just standards that shift – even the basic business models have shifted dramatically. When the OpenAccess Coalition was formed 8 years ago, traditional IDMs drove the requirements and supplied the initial resources. Cadence soon joined in with an unprecedented resource commitment, but only because these IDMs set the vision and drove the agenda first. OpenAccess would not exist today were it not for the leadership and ongoing resource investment of these IDMs – even though in current times every part of the supply chain now benefits from OpenAccess, and it has enabled a wave of innovation on top of it that creates more opportunity for our industry's success ahead.

This begs an important question: Who should be involved in developing standards? Eight years ago, the leading IDMs came together and "encouraged" their suppliers to engage with them, making OpenAccess possible. Today, however, many of those IDMs have gone fabless, and/or have shrunk in market clout to other fabless companies. These fabless design houses, along with their foundry and EDA partners, have quickly overtaken many traditional IDMs as the new market revenue leaders. Most of these newer fabless companies achieved their initial edge with a next-product "laser focus" that used available standards, but often minimized any investment in their creation or support. The problem is that the children have now become the parents, so to speak. Whose job is it now to invest in the future efficiency of our industry? Some industry observers claim that those who lead the industry in market revenues should also recognize that it is in their own best interest to take up the mantle and be leaders in standards development to enable a more efficient industry ahead.

Our industry has thrived through many dynamic transitions, and numerous significant EDA standards have been a key enabler for the industry's success. Going forward, the new market leaders must continue to invest in those standards upon which we economically and strategically depend for our business, including those emerging areas where effective standards can enable healthy growth for our industry and competitive advantage for those who recognize that vision.

**Steve Schulz
President & CEO, Si2**

Industry Events

3-D Architectures Conference (Si2 Co-Sponsors)

Dec. 8-10, Burlingame, CA: The key objective of the 2010 conference is to continue to provide this unique forum dedicated to serving the needs of the entire 3-D community. With invited speakers and participants from leading companies and organizations around the world, the conference aims to provide information critical to planning ongoing and future business and technical efforts impacted by 3-D integration and packaging. The presentation/proceedings format gives speakers the freedom to share the latest insights and information.

For more information on the conference: http://techventure.rti.org/Winter2010/

ICCAD 2010(Si2 - Corporate Sponsors)

Nov. 7-11, San Jose, CA: The International Conference on Computer-Aided Design (ICCAD) is the world's premier conference devoted to technical innovations in design automation of devices, circuits, and systems and has served EDA and Design professionals for the last 25 years by highlighting new challenges and breakthrough innovative solutions for integrated circuit design technologies and systems. ICCAD remains uniquely recognized as the place where the most in-depth and respected research work in EDA is presented. For more information, go to http://www.iccad.com/2010/index.html

Much of the information in this newsletter is the direct result of the extensive effort put forth by Si2 member companies in the many Working Groups in the various Coalitions. We extend our sincere appreciation for their contributions.

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